Bipolar Junction Transistors (BJT)
PNP & NPN (Emitter Base Collector)

Note: NPN’s are more commonly encountered due to greater ease of production.
Bipolar (majority and minority carriers)
Forward voltage characteristics of PN junction (approximately 0.2 volts for Ge and 0.7 volts for Si).

Biasing:

\[
\begin{align*}
\text{NPN} & \quad V_c > V_e \quad V_{be} = +0.7 \\
\text{PNP} & \quad V_e > V_c \quad V_{be} = -0.7
\end{align*}
\]

BJTs are current-controlled devices: Symbology and Voltage / Current Relationships:

- \( V_{BB} \) Base Bias Voltage
- \( V_{EE} \) Emitter Bias Voltage
- \( V_{CC} \) Collector Bias Voltage
- \( V_{be} \) Voltage drop across Emitter Base Junction
- \( V_{cb} \) Voltage drop across Collector Base Junction
- \( V_{ce} \) Voltage drop from Collector to Emitter

\[
\begin{align*}
I_e &= I_c + I_b \\
I_c &= \alpha I_e \\
I_c &= \beta I_b \\
I_c &= (1 + \beta) I_b \\
I_b &= (1 - \alpha) I_e \\
\beta &= \alpha(1 - \alpha) \\
\alpha &= \beta(1 + \beta) \\
\alpha &\approx 1 \quad \beta = 20 - 2000 \quad (100 - 400)
\end{align*}
\]

Three Regions of BJT operations and required biasing for each:

- **Active (Linear) {Amplification}**
  - Base Emitter Forward, Collector Base Reverse
- **Cut-Off {Open Switch - No Current Flow}**
  - Base Emitter Reverse, Collector Base Reverse
- **Saturation {Closed Switch - High Current Flow}**
  - Base Emitter Forward, Collector Base Forward

**Active Region**
Linear Amplification (High Fidelity - No Distortion)
- Emitter/Base Forward Bias
- Collector/Base Reverse Bias

**Cut-Off Region**
Both junctions reversed biased
- Emitter/Base voltage insufficient to cause emitter current flow
- Zero current (same as open switch)

**Saturation Region**
Both junctions forward biased
- Heavy current conduction (same as closed switch)

**Configurations and Characteristics:**

- **Common Base**
  - Unity Current Gain
  - High Voltage Gain
  - No phase shift

- **Common Emitter**
  - 180° Phase Shift
  - High Power Gain (Both High Current and High Voltage Gains)
  - Most frequently used configuration

- **Common Collector (Emitter Follower)**
  - Unity Voltage Gain
  - No phase shift
  - High Input Impedance & Low Output Impedance
**BJT Amplifiers**

<table>
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<td>Ideal</td>
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<td></td>
<td></td>
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<tr>
<td>Common Emitter</td>
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<td>Infinite</td>
<td>1 - 10K Ohm</td>
<td>1 - 10K Ohm</td>
<td>180°</td>
</tr>
<tr>
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<td>&gt; 1000</td>
<td>&lt; 1K Ohm</td>
<td>&lt; 1K Ohm</td>
<td>0°</td>
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<tr>
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<td>100 - 1000</td>
<td>&lt; Av</td>
<td>&lt; 10K Ohm</td>
<td>&gt; 10K Ohm</td>
<td>0°</td>
</tr>
</tbody>
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---

**Diagrams:**

(a) A common-emitter (CE) amplifier
(b) A common-collector (CC) amplifier
(c) A common-base (CB) amplifier

*Robert T. Paynter*

*Introductory Electronic Devices and Circuits: Electron Flow Version, 6e*
BJT Amplifier Configurations

Common Base-Biased BJT Amplifier

Base-Biased Common Emitter BJT Amplifier

Emitter-Biased Common Emitter BJT Amplifier

Emitter-Biased Common Collector BJT Amplifier
Transistor Switch

\[ V_{CC} +5 \text{ V} \]
\[ +1 \text{ k}\Omega \]
\[ V_{out} \]
\[ R_L \]
\[ V_{BE} \]
\[ V_{CE} \]
\[ \beta_{min} = 100 \]

The BJT Inverter

\[ V_{CC} +5 \text{ V} \]
\[ R_L \]
\[ I_C = 0 \]
\[ V_{out} = V_{CC} \]
\[ = 5 \text{ V} \]
\[ I_B = 0 \]

Transistor OFF

\[ V_{CC} +5 \text{ V} \]
\[ R_L \]
\[ I_C = 0 \]
\[ V_{out} = V_{CE(sat)} \]
\[ \leq 0 \text{ V} \]

Transistor ON

Switch

Open

(ON)
Field Effect Transistors (FET)

FET (JFET & MOSFET)

P-type & N-type (Source, Drain, Gate)

Unipolar (majority carriers only)

JFETs are voltage-controlled devices: \( v_o = a v_i \)

Forward Bias with respect Source & Drain

P Channel: Source + and Drain - (conventional current flow Source to Drain \( I_D \))

N Channel: Source - and Drain + (conventional current flow Drain to Source \( I_D \))

Reverse Bias with respect to Source & Gate (Max current flow \( I_D \) when \( V_{gs} = 0 \))

P Channel: Gate more positive than Source causes a decrease in \( I_D \) current flow

N Channel: Gate more negative than Source causes a decrease in \( I_D \) current flow

Terminology:

\( V_p \) (Pinch-Off Voltage)

The \( V_{DS} \) voltage at which the current \( I_D \) levels off \( (V_{GS} = 0) \)

\( I_{DSS} \) (Drain-Source Saturation Current)

Maximum current flow with \( V_{DS} > V_p \) and \( V_{GS} = 0 \).

\( V_{GS\,\text{off}} \) (Gate-to-Source Cutoff Voltage) Note: \( V_p = |V_{GS\,\text{off}}| \)

The value of \( V_{GS} \) which results in total channel depletion, and hence zero current flow \( (I_D = 0) \).

Quiescent (Operating Points)

\( I_{DQ} \)

\( V_{DSQ} \)

Equations:

Self Biased

\[
I_D = \frac{-V_{GS}}{R_s} \quad V_{DS} = V_{DD} - I_D \left( R_D + R_s \right)
\]

Voltage Divider

\[
I_D = \frac{V_G - V_{GS}}{R_s} \quad V_{DS} = V_{DD} - I_D \left( R_D + R_s \right)
\]
Field Effect Transistors (FETs)

**N-CHANNEL JFET**

**N-CHAN CURVES**

**P-CHANNEL JFET**

**P-CHAN CURVES**

**DRAIN CURRENT**

(OHMIC REGION)

\[ I_D = I_{DSS} \left[ 2 \left( 1 - \frac{V_{GS}}{V_{GSS,eff}} \right) \frac{V_{DS}}{V_{GSS,eff}} - \left( \frac{V_{DS}}{V_{GSS,eff}} \right)^2 \right] \]

**DRAIN CURRENT**

(ACTIVE REGION)

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GSS,eff}} \right)^2 \]

\[ R_{DS} = \frac{V_{DS}}{I_D} = \frac{V_{GSS,eff}}{2I_{DSS}(V_{GS} - V_{GSS,eff})} = \frac{1}{g_m} \]

\[ R_{DSS,\text{on}} = \text{constant} \]

\[ V_{DS} = V_D - V_S \]

**ON RESISTANCE**

**DRAIN-SOURCE RESISTANCE**

**VOLTAGE**

**TRANSCONDUCTANCE**

\[ g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{1}{R_{DS}} \]

\[ g_m = g_m \left( 1 - \frac{V_{GS}}{V_{GSS,eff}} \right) = g_m \sqrt{\frac{I_D}{I_{DSS}}} \]

\[ g_m = \frac{2I_{DSS}}{V_{GSS,eff}} \]

**TRANSCONDUCTANCE**

FOR SHORTED GATE

**OHMIC REGION**

JFET is just beginning to resist. It acts like a variable resistor.

**SATURATION REGION**

JFET is most strongly influenced by gate-source voltage, hardly at all influenced by the drain-source voltage.

**CUTOFF VOLTAGE** (\(V_{GSS,off}\)) Particular gate-source voltage where JFET acts like an open circuit (channel resistance is at its maximum).

**BREAKDOWN VOLTAGE** (\(BV_{DS}\)) The voltage across the drain and source that caused current to “break through” the JFET’s resistive channel.

**DRAIN-CURRENT FOR ZERO BIAS (\(I_{DS}^{\text{off}}\))** Represents the drain current when gate-source voltage is zero volts (or gate is connected to source, \(V_{GS} = 0\) V).

**TRANSCONDUCTANCE** (\(g_m\)) Represents the rate of change in the drain current with the gate-source voltage when the drain-to-source voltage is fixed for a particular \(V_{DS}\). It is analogous to the transconductance (\(1/R_{DSS}\)) for bipolar transistors.

**Typical JFET values:**

\(I_{DSS}^{\text{1 mA to 1 A}}\)

\(V_{GSS,off}^{\text{–0.5 to –10 V (n-channel)}}\)

\(0.5 \text{ to } 10 \text{ V (p-channel)}\)

\(R_{DSS,\text{on}}^{\text{10 to 1000 \Omega}}\)

\(BV_{DS}^{\text{6 to 50 V}}\)

\(g_m\) at 1 mA:

500 to 3000 \(\mu\text{mho}\)

Practical Electronics for Inventors
Figure 7-8: Plot of Drain and Transfer Characteristics for an n-channel JFET

(b) Transfer Characteristics

(a) Drain Characteristics

Figures 7-6, 7, 8. Kazimierczuk Electronic Devices

Source: Electronic Devices a design approach. Ali Aminian and Marian Kazimierczuk, 2004
Junction Field Effect Transistors JFET

Three Terminals: Drain, Source, Gate

Majority Carriers Only (Unipolar)
  N Channel  Electrons

By convention, always draw with **Drain** at the top

N Type Channel Arrow Pointing **IN**

Forward Bias Source to Drain **V\_DD**

  For N Channel
  + to Drain
  - to Source

Conventional Current Flow **I\_D** (From Drain to Source)

Reverse Bias Gate to Source  **I\_G = 0**

  - to Gate
  + to Source

**V\_G** is the Gate to Ground Voltage
**V\_GS** is the Gate to Source Voltage

**V\_P** (Pinch-Off Voltage)  The **V\_DS** voltage at which the current **I\_D** levels off (for **V\_GS = 0**)

**V\_GS**(off) (Gate-to-Source Cutoff Voltage **I\_D = 0**)  **V\_P = |V\_GS**(off)** |

**I\_DSS** (Drain-Source Saturation Current)  Maximum current flow with **V\_GS = 0**.

Quiescent (Operating Points)

\[
I\_DQ  \\
V\_DSQ
\]

Shockley's Equation

\[
I\_D = I\_DSS \left( 1 - \frac{V\_GS}{V\_GS**(off)} \right)^2
\]

Notes:

**V\_GS** and **V\_GS**(off) are always the same algebraic sign, so **V\_GS / V\_GS**(off) will always be positive.

For N Channel, **V\_GS**(off) is negative, **V\_P = |V\_GS**(off)** |
\[
\text{so } I\_D = I\_DSS \left( 1 + \frac{V\_GS}{V\_P} \right)^2
\]

Biasing N Channel JFETs  i.e., calculating Quiescent (Operating Points), **I\_DQ** and **V\_DSQ**

**I\_DSS** and **V\_GS**(off) are from readily obtainable from Transfer Characteristics Charts

For Fixed Biased, **V\_GS = V\_GG** (since reversed bias, **I\_G = 0**, **V\_RG = 0**, **V\_GS = V\_GG**)

For Self Biased and Voltage Divider Biased, **V\_GS** is the solution of a quadratic equation.
For BME 3512, **I\_DSS**, **V\_GS**(off), **V\_GS** will be given.
Fixed Biased

\[ I_{DSS} = 12 \text{ mA} \quad V_{GS(off)} = -4 \text{ V} \]

Given: \( I_{DSS} = 12 \text{ mA} \quad V_{GS(off)} = -4 \text{ V} \)

Since Gate to Source is reverse biased, \( I_G = 0 \), hence \( V_{Gg} = I_G R_g = 0 \)

And \( V_{GG} = I_G R_g + V_{GS} \)

\[ V_{GG} = 0 + V_{GS} \]

\[ V_{GS} = V_{GG} = -1 \text{ V} \]

From Shockley's Equation

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 = 12 \times 10^{-3} \times \left( 1 - \frac{-1}{-4} \right)^2 = 6.75 \text{ mA} \]

\[ V_{DD} = V_{DS} + I_D R_D \rightarrow V_{DS} = V_{DD} - I_D R_D = 12 - 6.75 \times 10^{-3} \left( 1 \times 10^{-3} \right) = 5.25 \text{ V} \]

Answers: \( I_{DQ} = 6.8 \text{ mA} \) and \( V_{DSQ} = 5.3 \text{ V} \)
Examples Biasing N Channel JFETs  Determine Quiescent (Operating Points), $I_{DQ}$ and $V_{DSQ}$

Self-Biased

$I_{DSS} = 16 \text{ mA} \quad V_{GS(\text{off})} = -4 \text{ V}$

![Diagram of a self-biased circuit](image)

A self-biased circuit

Given: $I_{DSS} = 16 \text{ mA} \quad V_{GS(\text{off})} = -4 \text{ V} \quad V_{GS} = \text{see below}$

The $I_D$ current through $R_S$ will develop a voltage across $R_S$ such that the Source is at a positive potential with respect to Ground. If any current $I_G$ flows at all, the Gate will be at a negative potential with respect to Ground and hence the Gate to Source will be reversed bias resulting in $I_G = 0$, hence $V_{RG} = I_G R_g = 0$, and therefore $V_G$ (Gate to Ground) = 0.

But $V_G = V_{GS} + I_D R_S$

$0 = V_{GS} + I_D R_S$

$I_D = -V_{GS} / R_S$

From $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$ and $I_D = -V_{GS} / R_S \Rightarrow \frac{-V_{GS}}{R_S} = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$

Solve for $V_{GS}$ (see page 5 Summary of FET Biasing Equations) Note:

For BME 3512 the value of $V_{GS}$ will be given. $V_{GS} = -2.44 \text{ V}$

$I_D = -V_{GS} / R_S = (-2.44) / 1 \times 10^3 = 2.44 \text{ mA}$

$V_{DD} = V_{DS} + I_D (R_D + R_S) \Rightarrow V_{DS} = V_{DD} - I_D (R_D + R_S) = 15 - 2.44 \times 10^{-3} (1500 + 1000) = 8.9 \text{ V}$

Answers: $I_{DQ} = 2.4 \text{ mA}$ and $V_{DSQ} = 8.9 \text{ V}$
**Voltage Divider Biased**

Given: $I_{DSS} = 12 \text{ mA}$  \hspace{1cm} $V_{GS(\text{off})} = -3 \text{ V}$  \hspace{1cm} $V_{GS} = \text{see below}$

From the voltage divider network:

$$V_{G} = V_{DD} \frac{R_2}{R_1 + R_2}$$

By definition:

$$V_{GS} = V_{G} - V_{S} = V_{G} - I_{D}R_{SS}$$

Hence

$$I_{D} = \left( V_{G} - V_{GS} \right) / R_{S}$$

From $I_{D} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$ and $I_{D} = \left( V_{G} - V_{GS} \right) / R_{S}$

$$\frac{V_{G} - V_{GS}}{R_{S}} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2$$

Solve for $V_{GS}$ (see page 5 Summary of FET Biasing Equations)

Note: For BME 3512 the value of $V_{GS}$ will be given. $V_{GS} = -1.31 \text{ V}$

$$V_{G} = V_{DD} \frac{R_2}{R_1 + R_2} = 15 \frac{150K}{750K+150K} = 2.50 \text{ V}$$

$$I_{D} = \left( V_{G} - V_{GS} \right) / R_{S} = [2.5 - (-1.31)] / 1000 = 3.81 \text{ mA}$$

$$V_{DS} = V_{DD} - I_{D} (R_D + R_S) = 15 - 3.81 \times 10^{-3} (1500 + 1000) = 5.48 \text{ V}$$

Answers: $I_{DQ} = 3.8 \text{ mA}$ and $V_{DSQ} = 5.5 \text{ V}$
Summary of Equations for the Analysis of Self-Biased and Voltage-Divider Biased JFET Amplifier

Self-bias:

\[ V_{GS_{n-channel}} = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \]

\[ V_{GS_{p-channel}} = \frac{+b - \sqrt{b^2 - 4ac}}{2a} \]

where,

\[ a = \frac{I_{DSS}R_S}{V_p^2} \]

\[ b = \frac{2I_{DSS}R_S}{|V_p|} + 1 \]

\[ c = I_{DSS}R_S \]

\[ I_D = \frac{-V_{GS}}{R_S} \]

\[ V_{DS} = V_{DD} - I_D(R_D + R_S) \]

Voltage-divider bias:

\[ V_{GS_{n-channel}} = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \]

\[ V_{GS_{p-channel}} = \frac{+b - \sqrt{b^2 - 4ac}}{2a} \]

where,

\[ a = \frac{I_{DSS}R_S}{V_p^2} \]

\[ b = \frac{2I_{DSS}R_S}{|V_p|} + 1 \]

\[ c = I_{DSS}R_S - |V_G| \]

\[ I_D = \frac{V_G - V_{GS}}{R_S} \]

\[ V_{DS} = V_{DD} - I_D(R_D + R_S) \]

Source: Electronic Devices a design approach. Ali Aminian and Marian Kazimierczuk, 2004