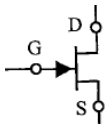
Junction Field Effect Transistors JFET

Three Terminals: Drain, Source, Gate

Majority Carriers Only (Unipolar)
N Channel Electrons

By convention, always draw with **Drain** at the top



N Type Channel Arrow Pointing **IN**

Forward Bias Source to Drain V_{DD}

For N Channel
+ to Drain
- to Source
Conventional Current Flow I_D (From Drain to Source)

Reverse Bias Gate to Source $I_G = 0$
- to Gate
+ to Source

V_G is the Gate to Ground Voltage
V_{GS} is the Gate to Source Voltage

V_P (Pinch-Off Voltage) The V_{DS} voltage at which the current I_D levels off (for $V_{GS} = 0$)

$V_{GS(off)}$ (Gate-to-Source Cutoff Voltage $I_D = 0$) $V_P = |V_{GS(off)}|$

I_{DSS} (Drain-Source Saturation Current) Maximum current flow with $V_{GS} = 0$.

Quiescent (Operating Points)

I_{DQ}

V_{DSQ}

Shockley's Equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Notes:

V_{GS} and $V_{GS(off)}$ are always the same algebraic sign, so $V_{GS} / V_{GS(off)}$ will always be positive.

For N Channel, $V_{GS(off)}$ is negative, $V_P = |V_{GS(off)}|$, so $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$

Biasing N Channel JFETs i.e., calculating Quiescent (Operating Points), I_{DQ} and V_{DSQ}

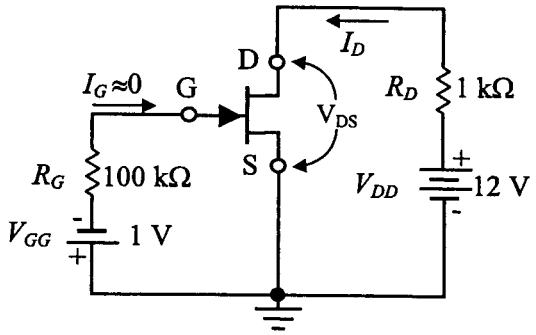
I_{DSS} and $V_{GS(off)}$ are from readily obtainable from Transfer Characteristics Charts

For Fixed Biased, $V_{GS} = V_{GG}$ (since reversed bias, $I_G = 0$, $V_{RG} = 0$, $V_{GS} = V_{GG}$)

For Self Biased and Voltage Divider Biased, V_{GS} is the solution of a quadratic equation.
For BME 3512, I_{DSS}, $V_{GS(off)}$, V_{GS} will be given.

Fixed Biased

I_{DSS} = 12 mA $V_{GS(off)} = -4$ V



A fixed bias circuit

Given: I_{DSS} = 12 mA $V_{GS(off)}$ = -4 V

Since Gate to Source is reverse biased, $I_G = 0$, hence $V_{Rg} = I_G R_g = 0$

And $V_{GG} = I_G R_g + V_{GS}$

$V_{GG} = 0 + V_{GS}$

$V_{GS} = V_{GG} = -1$ V

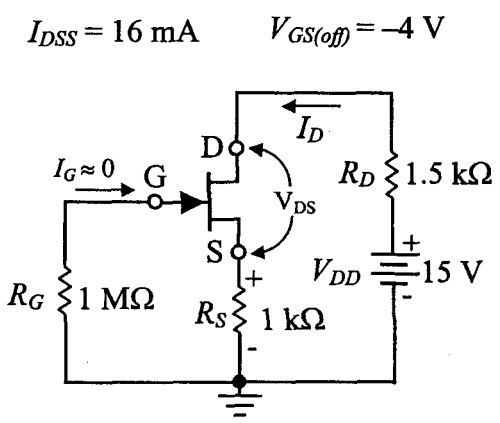
From Shockley's Equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 12\times10^{-3}\times\left(1 - \frac{-1}{-4}\right)^2 = 6.75 \text{ mA}$$

$$V_{DD} = V_{DS} + I_D R_D \rightarrow V_{DS} = V_{DD} - I_D R_D = 12 - 6.75\times10^{-3}\left(1\times10^{-3}\right) = 5.25 \text{ V}$$

Answers: I_{DQ} = 6.8 mA and V_{DSQ} = 5.3 V

Self-Biased



A self-biased circuit

Given: I_{DSS} = 16 mA $V_{GS(off)}$ = - 4 V V_{GS} = see below

The I_D current through R_S will develop a voltage across R_S such that the Source is at a positive potential with respect to Ground. If any current I_G flows at all, the Gate will be at a negative potential with respect to Ground and hence the Gate to Source will be reversed bias resulting in
$I_G = 0$, hence $V_{Rg} = I_G R_g = 0$, and therefore V_G (Gate to Ground) = 0.

But $V_G = V_{GS} + I_D R_S$

$0 = V_{GS} + I_D R_S$

$I_D = -V_{GS} / R_S$

From $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$ and $I_D = -V_{GS} / R_S$ $\rightarrow$ $\frac{-V_{GS}}{R_S} = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

Solve for V_{GS} (see page 5 Summary of FET Biasing Equations)

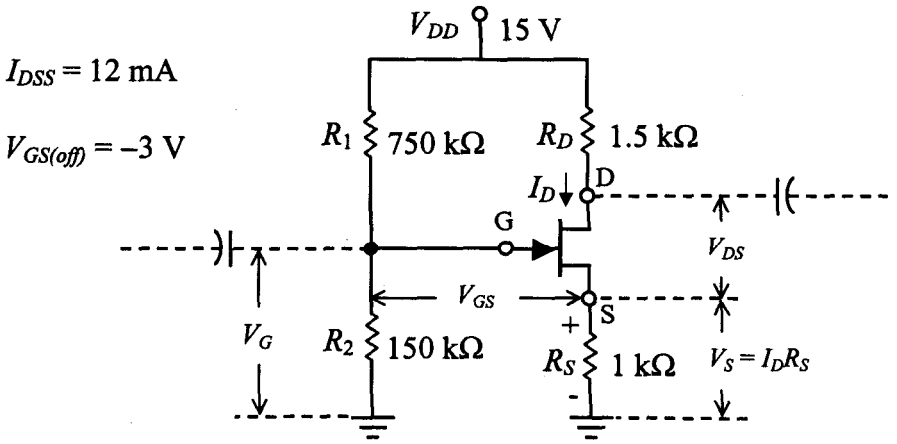
Note: For BME 3512 the value of V_{GS} will be given. V_{GS} = - 2.44 V

$I_D = -V_{GS} / R_S$ = - (-2.44) / 1 x 10^3 = 2.44 V

$$V_{DD} = V_{DS} + I_D(R_D + R_S) \rightarrow V_{DS} = V_{DD} - I_D(R_D + R_S) = 15 - 2.44\times10^{-3}(1500 + 1000) = 8.9 \text{ V}$$

Answers: I_{DQ} = 2.4 mA and V_{DSQ} = 8.9 V

Voltage Divider Biased



A voltage-divider biased JFET amplifier circuit

Given: I_{DSS} = 12 mA $V_{GS(off)}$ = - 3 V V_{GS} = see below

From the voltage divider network: $V_G = V_{DD} \dfrac{R_2}{R_1 + R_2}$

By definition: $V_{GS} = V_G - V_S = V_G - I_D R_{SS}$

Hence $I_D = (V_G - V_{GS}) / R_S$

From $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)^2$ and $I_D = (V_G - V_{GS}) / R_S$ ➡ $\dfrac{V_G - V_{GS}}{R_S} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)^2$

Solve for V_{GS} (see page 5 Summary of FET Biasing Equations)

Note: For BME 3512 the value of V_{GS} will be given. V_{GS} = - 1.31 V

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 15 \frac{150\,\text{K}}{750\,\text{K} + 150\,\text{K}} = 2.50\ \text{V}$$

$I_D = (V_G - V_{GS}) / R_S = [2.5 - (-1.31)] / 1000 = 3.81$ mA

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 15 - 3.81 \times 10^{-3}(1500 + 1000) = 5.48\ \text{V}$$

Answers: I_{DQ} = 3.8 mA and V_{DSQ} = 5.5 V

Summary of Equations for the Analysis of Self-Biased and Voltage-Divider Biased JFET Amplifier

Self-bias:

$$V_{GS}\Big|_{n-channel} = \frac{-b+\sqrt{b^2-4ac}}{2a}$$

$$V_{GS}\Big|_{p-channel} = \frac{+b-\sqrt{b^2-4ac}}{2a}$$

where,

$$a = \frac{I_{DSS}R_S}{V_P^{\,2}} \qquad b = \frac{2I_{DSS}R_S}{|V_P|}+1 \qquad c = I_{DSS}R_S$$

$$I_D = \frac{-V_{GS}}{R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Voltage-divider bias:

$$V_{GS}\Big|_{n-channel} = \frac{-b+\sqrt{b^2-4ac}}{2a}$$

$$V_{GS}\Big|_{p-channel} = \frac{+b-\sqrt{b^2-4ac}}{2a}$$

where,

$$a = \frac{I_{DSS}R_S}{V_P^{\,2}} \qquad b = \frac{2I_{DSS}R_S}{|V_P|}+1 \qquad c = I_{DSS}R_S - |V_G|$$

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Source: Electronic Devices a design approach. Ali Aminian and Marian Kazimierczuk, 2004