Microelectronics/MEMS

- How are they made?
- What are they made out of?
- How do their materials behave?

Wires

Transistors
Diodes
Resistors
Capacitors
Course Outline

- Semiconductor Materials
- Crystal structure, growth, & epitaxy
- Film formation – oxidation & deposition
- Metalization
- Lithography & etching
- Impurity doping – diffusion & implantation
- Lithography
- Etching
- Resistivity Measurement
- Other Techniques
Semiconductor Materials

- Material Classes
  - Solid
    - Insulators
    - Semiconductors
    - Conductors
  - Liquid
  - Gas

2-D schematic representation of crystalline solids, amorphous materials or liquids, and gases.

Solids

General classification of solids based on the degree of atomic order

- Semiconductors are sensitive to:
  - Temperature, photon flux (illumination), magnetic field, pressure
  - Variability controlled by selectively adding impurities on the order of 1ppm
- **Lattice** – the periodic arrangement of atoms in a crystal
### Compound Semiconductors

**NOTE:** We will concentrate primarily on Si - most common MEMS material

#### Reasons for Silicon usage:
- Room Temp performance - good
- High quality silicon dioxide
- Grown thermally
- Reduced cost
- 2nd most abundant element on earth
  - Oxygen first
- Earth’s crust
  - Silica & silicates
  - 25%

#### Compound semiconductor usage:
- Binary
- Ternary
- Quaternary
- Better electrical & optical properties
- Good for
  - High-speed electronics
  - Photonic devices

<table>
<thead>
<tr>
<th>Element</th>
<th>Symbol</th>
<th>Name</th>
<th>Group</th>
<th>Compound Structure</th>
<th>Applications</th>
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<tbody>
<tr>
<td>Si</td>
<td>Si</td>
<td>Silicon</td>
<td>III</td>
<td>Ge</td>
<td>High-speed electronics, Photonic devices</td>
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<td>Ge</td>
<td>Germanium</td>
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<td>Al</td>
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<td>III</td>
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<td>GaP, GaAs</td>
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<tr>
<td>Pb</td>
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<td>IV</td>
<td>PbS</td>
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</tr>
<tr>
<td>Bi</td>
<td>Bi</td>
<td>Bismuth</td>
<td>III</td>
<td></td>
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</tbody>
</table>

**Crystal Structure**

- Arrangement of atoms that define a particular material
- 3 Categories
  - Amorphous – density varies, no unique pattern
  - Crystalline – one region defines all regions
  - Polycrystalline – sets of crystalline regions with boundaries

- Elemental semiconductors (column IV)
  - Ex. Si ≡ SiO₂ – very stable oxide (hydrophobic) moderate n_i
    - Ge ≡ oxides are solvable to H₂O – large leakage currents as Temp ↑
- Compound Semiconductors (column III-V, II-VI, etc)
  - Ex. GaAs ≡ no stable oxide but direct bandgap
    - Applications: microwave and photonic devices
Simple unit cells

- Unit Cell – a representative of the entire lattice
  - By repeating unit cell throughout the crystal, one can recreate the entire lattice

A generalized primitive unit cell.

Simple examples of unit cells come from the family of 14 Bravais lattices

- simple cubic (sc) = polonium
- bcc = Na, W
- fcc = Al, Cu, Au, Pt, large number of elements exhibit this lattice form

Ex. - Problem

1) Determine # of atoms in each cubic structure – sc, bcc, fcc?
2) Find fraction of filled cell of an fcc?
Diamond Structure

- Lattice – fcc
- Basis – two C atoms at (0,0,0) and (1/4,1/4,1/4) associated with each fcc lattice point
- 8 atoms in conventional unit cell
- Two interpenetrating fcc sublattice with one sublattice displaced by 1/8 of the distance along the body diagonal of the cube (displacement of $a\sqrt{2}/4$)

Figure 2.4. (a) Diamond lattice. (b) Zincblende lattice.

<table>
<thead>
<tr>
<th>ELEMENT</th>
<th>CUBE SIDE $a$ (Å)</th>
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<tbody>
<tr>
<td>C (diamond)</td>
<td>3.57</td>
</tr>
<tr>
<td>Si</td>
<td>5.43</td>
</tr>
<tr>
<td>Ge</td>
<td>5.66</td>
</tr>
<tr>
<td>α-Sn (grey)</td>
<td>6.49</td>
</tr>
</tbody>
</table>

Zinc Blende or Sphalerite Lattice

- Bravais lattice – fcc
  - Ex – cubic zinc sulfide structure
  - Basis – Zn (0,0,0) & S (1/4,1/4,1/4)
  - Two interpenetrating fcc lattices
    - One composed entirely of Zn
    - Other of S, offset by 1/4 of a cubic diagonal

Zincblende lattice.
- Most III-V compound semiconductors have zincblende lattice
- Identical to diamond (one fcc from column III, other from V) – Ex. GaAs

<table>
<thead>
<tr>
<th>CRYSTAL</th>
<th>$a$ (Å)</th>
<th>CRYSTAL</th>
<th>$a$ (Å)</th>
<th>CRYSTAL</th>
<th>$a$ (Å)</th>
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<tr>
<td>CuF</td>
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<td>ZnS</td>
<td>5.41</td>
<td>AlSb</td>
<td>6.13</td>
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<td>CuCl</td>
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<td>ZnSe</td>
<td>5.67</td>
<td>GaP</td>
<td>5.45</td>
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<tr>
<td>CuBr</td>
<td>5.69</td>
<td>ZnTe</td>
<td>6.09</td>
<td>GaAs</td>
<td>5.65</td>
</tr>
<tr>
<td>CdI</td>
<td>6.04</td>
<td>CdS</td>
<td>5.82</td>
<td>GaS</td>
<td>6.12</td>
</tr>
<tr>
<td>AgI</td>
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<td>CdTe</td>
<td>6.48</td>
<td>InP</td>
<td>5.87</td>
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<tr>
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<td>HgS</td>
<td>5.85</td>
<td>InAs</td>
<td>6.04</td>
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<tr>
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<td>5.07</td>
<td>HgSe</td>
<td>6.08</td>
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<td>6.48</td>
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<tr>
<td>BeTe</td>
<td>5.34</td>
<td>HgTe</td>
<td>6.43</td>
<td>SiC</td>
<td>4.35</td>
</tr>
<tr>
<td>MoS (w)</td>
<td>5.60</td>
<td>AlP</td>
<td>5.43</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MoSe</td>
<td>5.82</td>
<td>AlAs</td>
<td>5.62</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Simplified Lattice Representation

The lattice mismatch, or misfit, is defined as

$$\Delta a = \frac{a - a_0}{a}$$

Could be substrate $a$ or the average $a$ of two or more epitaxial/substrate layer(s)

Accommodation of lattice of epitaxial layer with that of substrate for different cases: (a) lattice-matched growth ($a=a_0$), (b) biaxial compressive strain ($a>a_0$), and (c) biaxial tensile strain ($a<a_0$)

Miller Indices

Cubic lattices \((hkl)\) ≡ crystal plane

A convenient method of defining the various planes in a crystal is to use Miller indices. These indices are obtained using the following steps:

1. Find the intercepts of the plane on the three Cartesian coordinates in terms of the lattice constant
2. Take the reciprocals of these numbers and reduce them to the smallest three integers having the same ratio
3. Enclose the result in parentheses \((hkl)\) as the Miller indices for a single plane

Used to define planes & directions in a crystal lattice

\((hkl)\) plane that intercepts reciprocals of indices
\(<hkl>\perp (hkl)\) plane
\([hkl]\) – specific direction
\(\{hkl\}\) – sets of equivalent planes
\(<hkl>\) – sets of equivalent directions

Figure 2.5. A \((623)\)-crystal plane.
Miller Indices - Examples

Miller indices of some important planes in a cubic crystal.

Semiconductor/MEMS Device Fabrication

- Fabricated through a series of repeated steps of
  - Oxidation
  - Photolithography
  - Etching
  - Diffusion
  - Evaporation or sputtering
  - Chemical vapor deposition (CVD)
  - Ion implantation
  - Epitaxy
  - Annealing
Crystal Growth - Si

Si crystal growth from the Melt
➢ 90% Si crystals grown with Czochralski
➢ Pure form of sand (SiO₂) – quartzite

\[ \text{SiCl}_4(s) + \text{SiO}_2(s) \rightarrow \text{Si}(s) + \text{SiO}(g) + \text{CO}(g) \]

➢ Results in metallurgical grade Si – 98% pure

➢ Si pulverized & treated with HCl to form trichlorosilane

\[ \text{Si}(s) + 3\text{HCl}(g) \xrightarrow{300^\circ C} \text{SiHCl}_3(g) + \text{H}_2(g) \]

➢ Trichlorosilane liquid at RT. Fractional distillation of liquid removes unwanted impurities

➢ Purified SiHCl₃ used in hydrogen reduction to prepare the electronic-grade Si

\[ \text{SiHCl}_3(g) + \text{H}_2(g) \rightarrow \text{Si}(s) + 3\text{HCl}(g) \]

➢ Pure EGS – impurity concentrations in parts/Billion
**Basic Crystal Growth Technique**

- Crucible heated by RF induction or thermal resistance
- Melting pt – 1412 deg C
- Crucible rotates
  - Prevents formation of local hot/cold regions
- Argon backfilled
- Seed crystal – used to initiate the growth of the ingot with correct crystal orientation
- Pulled until Si in crucible depleted

**Czochralski Technique**

Pull rate – few mm/min (ex. 2mm/min = 4.7 in. in 1hr)
Magnetic field used for large ingots
- to control concentration of defects, impurities and oxygen content
Crystal diameter controlled by thermal input & pull rate
EGS also produced by the pyrolysis of silane (CVD reactor at 900°C) – lower cost & less toxic byproducts

\[ \text{SiH}_4(g) + \text{heat} \rightarrow \text{Si}(s) + 2\text{H}_2(g) \]
Distribution of Dopant

For Si – most common dopants
- Boron – p-type
- Phosphorous – n-type

As crystal is pulled from melt, dopant concentration in solid is usually different than the melt at the interface. Ratio of these two concentrations is defined as the equilibrium segregation coefficient $k_o$

$$k_o \equiv \frac{C_s}{C_l}$$  \hspace{1cm} (4)

where $C_s$ and $C_l$ are concentrations of solute (by weight) in solid and liquid.

<table>
<thead>
<tr>
<th>Table 1: Equilibrium Segregation Coefficients for Dopants in Si</th>
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<tbody>
<tr>
<td>Dopant</td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td>Al</td>
</tr>
<tr>
<td>Ga</td>
</tr>
<tr>
<td>In</td>
</tr>
<tr>
<td>O</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>P</td>
</tr>
</tbody>
</table>

*Deep-lying impurity level.

Float Zone Process

- Ideal for crystal purification
- High purity cast polysilicon rod
- A small zone (~ few cm) is heated by RF heater
- Floating zone traverses rod – molten Si is held in place by surface tension
- No contamination from crucible

![Image](image1.png)

**Figure 10.6.** Float-zone process. (a) Schematic setup. (b) Simple model for doping evaluation.

![Image](image2.png)

**Figure 10.8.** Relative impurity concentration versus zone length for a number of passes. $L$ denotes the zone length.
Material Characterization – Wafer shaping

- Remove seed with diamond saw
- Grind exterior surface to establish desired diameter
- Grind “flats” along ingot
  - Planes (crystal orientation and doping type)
- **Primary flat** - used as mechanical locator for subsequent processing steps
- **Secondary flats** – identify orientation & conductivity type
- Slice wafer with diamond saw
  - Surface orientation [<111> & <100> common for Si]
  - Thickness [0.5 to 0.7 mm]
  - Taper – thickness variations across wafer
  - Bow – curvature variation from center to edge
- Mechanical lapping/polishing
  - Polish one or both sides of wafer
  - Lapped using mixture of Al₂O₃ & glycerine
  - Flatness uniformity within 2 µm

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**Wafer Identification**

![Diagram of wafer identification](image)

**Figure 10.13.** Identifying flats on a semiconductor wafer.

<table>
<thead>
<tr>
<th>TABLE 3</th>
<th>Specification for Polished Monocrystal Silicon Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>125 mm</td>
</tr>
<tr>
<td>Diameter (mm)</td>
<td>125±1</td>
</tr>
<tr>
<td>Thickness (µm)</td>
<td>0.58–0.68</td>
</tr>
<tr>
<td>Primary flat length (mm)</td>
<td>80–95</td>
</tr>
<tr>
<td>Secondary flat length (mm)</td>
<td>25–30</td>
</tr>
<tr>
<td>Bow (µm)</td>
<td>70</td>
</tr>
<tr>
<td>Total thickness variation (µm)</td>
<td>55</td>
</tr>
<tr>
<td>Surface orientation</td>
<td>(100) ± 1°</td>
</tr>
<tr>
<td>(111) ± 1°</td>
<td>Same</td>
</tr>
</tbody>
</table>

*NA: Not available.*
Crystal Characterization

- Real crystals are not perfect – they have defects – two types
- Localized
  - Point defect – any foreign atom incorporated into the lattice structure either a substitutional site or an interstitial site
  - Missing atoms (host atoms)
  - Frenkel defect – host atom is situated between regular lattice sites & adjacent to a vacancy
- Non-Localized
  - Line – an extra or incomplete plane results in an edge dislocation
  - Area
    • Twinning – change in the crystal orientation across a plane
    • Grain boundary – transition region between single-crystal regions within a polycrystalline material
  - Volume – impurities or dopants migrate to form a specific high concentration region
    • Precipitates of impurities cause dislocations because of atom size mismatch
- Some defects can be removed by high temperature anneals

Crystal Defects

Figure 10.15. Point defects. (a) Substitutional impurity. (b) Interstitial impurity. (c) Lattice vacancy. (d) Frenkel-type defect.

Figure 10.16. (a) Edge and (b) screw dislocation formation in cubic crystals.
**Film Formation**

- Ceramic comb support
- Resistance heater
- Filtered air
- Silicon wafers
- To vent
- End cap (quartz)
- Fused quartz boat
- Exhaust

Example: LED/VCSEL

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**Epitaxy**

- Substrate wafer acts as the seed crystal
- The regular oriented growth of a single crystal layer(s) with controlled thickness and doping over a similar single crystal called the substrate
- Originally used to make high quality materials with characteristics superior to those of substrates
- Today, epitaxial techniques are used for the synthesis of ultra thin layers (monolayers), precise doping profiles or uniformity, and variable material compositions – in addition to low defect density material
- Enhances performance of devices and opens up many new possibilities
- Epitaxy processes occur at temps 30-50% lower than the melting pt.
- Types of epitaxial processes:
  - Vapor phase epitaxy (VPE) – metalorganic vapor phase epitaxy (MOVPE)
  - Liquid phase epitaxy (LPE) – rarely used
  - Molecular beam epitaxy (MBE) – MOMBE, gas source MBE (GSMBE), atomic layer epitaxy (ALE)
**Vapor Phase Epitaxy (VPE)**

- Also called CVD – chemical-vapor deposition
- **Epi growth** by vapor transport of reactants
- **Precursors** – are mixed with a “carrier gas” (i.e. H₂) which dilutes the mixer
- The gas, with its proportionate constituents, flows over or toward a heated substrate
- Some of the precursors are “cracked” into atom/molecule fragments while diffusing toward substrate surface (GaH₂ gas)
- **At the surface**, the atoms move to an appropriate lattice site and incorporate – else they recombine with other fragments
- Stagnant boundary layers form above the substrate from which reactant atoms/molecules diffuse to the substrate surface

**VPE Advantages/Disadvantages**

**Advantages**
- Low temperature process
- High purity (low defect density) material
- Readily automated for mass production
- Ability to grow thin layers with precise composition, doping density, thickness on an atomic scale for advanced systems
- Well suited to research – has opened “new” physics

**Disadvantages**
- Toxic gases are used – must have gas monitors and stainless steel plumbing. The exhaust pump system includes a ‘scrubber’ that breaks down toxic end products before atmospheric release (burn the gases)
- Research systems are expensive, as are many of the precursors (purchased as pressurized gases in cylinders or as ‘bubbler’s’)
- VPE works well with Si and GaAs (usually not used) – and related elemental and compound semiconductors
Silicon VPE

- Four silicon sources precursors:
  - $SiCl_4$: Silicon tetrachloride – most studied
  - $SiH_2Cl_2$: dichlorosilane
  - $SiHCl_3$: trichlorosilane
  - $SiH_4$: silane

- Typical reaction temp is 1200°C

Overall reaction:

$SiCl_4(gas) + 2H_2(gas) \rightarrow Si(solid) + 4HCl(gas)$

$SiCl_4(gas) + Si(solid) \rightarrow 2SiCl_4(gas)$

- Reversible reaction deposit or etch

Figure 10.20. Three common susceptors for chemical vapor disposition: (a) horizontal, (b) pancake, and (c) barrel susceptor.

MBE Thickness Uniformity

**THICKNESS UNIFORMITY**

**[a] WITHOUT ROTATION**

**[b] WITH ROTATION**

*FIGURE 4. Measurement of the Si layer deposition uniformity across a 3-in. substrate with and without rotation (after Ref. 18).*
Defects in Epitaxial Layers

- **Homoepitaxial growth**
  - Single-crystal semiconductor layer grown on a single-crystal semiconductor substrate.
  - Semiconductor layer and substrate are the same material – same lattice constant
  - Lattice matched epitaxial process

- **Heteroepitaxy** – epi layer and substrate are two different materials
  - Epi-layer must be grown such that the idealized interfacial structure is maintained
  - Atomic bonding across the interface must be continuous without interruption
  - Materials must have same lattice spacing or be able to deform to adopt a common spacing

  - Cases referred to as
    - Lattice-matched epitaxy
    - Strained-layer epitaxy

Schematic illustration of (a) lattice-matched, (b) strained, and (c) related heteroepitaxial structures. Homoepitaxy is structurally identical to the lattice-matched heteroepitaxy.

Epitaxy Defects - Strained Layer Epitaxy

- Defects degrade device properties – reduced mobilities, increased leakage currents

**Defect categories**

- 1) defects from substrates – may propagate from substrate into epi layer – must begin with defect-free substrates
- 2) defects from interface – oxide precipitates or contamination can cause misoriented clusters or stacking faults – thoroughly clean or reversible etch
- 3) precipitates or dislocation loops – due to supersaturation of impurities or dopants
- 4) Edge dislocations – formed in the heteroepitaxy of two lattice-mismatched semiconductors.
**Oxidation & Film Deposition**

- The creation of non-crystalline films used for non-semiconductor behavior
- Current conduction or isolation
- IC fabrication requires many types of films
  - Thermal oxides – highest quality
  - Dielectric layers – lower quality
  - Polycrystalline films
  - Metal films

![Schematic cross section of a metal-oxide-semiconductor field-effect transistor (MOSFET).](image)

**Thermal oxides**
- Gate oxide (establish the source to drain conducting channel)
- Wet oxidation results in rapid growth but the resultant oxide is very porous (gaps in the amorphous SiO₂ crystal)
- Dry oxidation results in a slower growth rate but higher density & smaller defect (traps/interface states) density SiO₂ \[\rightarrow\] best quality

**Field oxide**
- Isolation of similar devices on the substrate. High quality oxides with low impurity densities are required to minimize leakage currents
- Mask for diffusion/implants
- Surface passivation (CVD)

**Dielectric layers**
- Deposited SiO₂ and Si₃N₄
- Used for insulation between conductors, as an ion implantation mask, or as passivation layer(s)

**Polycrystalline silicon (Poly)**
- Serves as a gate electrode or a conductive material for multi-level metallizations

**Metal films**
- Al, silicides, Au for low resistance interconnects/bonding pads

**General requirements**
- Be definable by lithography and etching
- Perform function and be compatible chemically and physically with the surface below, and any surface applied above
Growth Mechanism and Kinetics

Dry
\[ \text{Si (solid)} + \text{O}_2 \text{ (gas)} \rightarrow \text{SiO}_2 \text{ (solid)} \]

Wet/steam
\[ \text{Si (solid)} + 2\text{H}_2\text{O} \text{ (gas)} \rightarrow \text{SiO}_2 \text{ (solid)} + 2\text{H}_2 \text{ (gas)} \]

- In order for the oxidizing species to reach the Si/SiO₂ interface and “grow” the oxide
  - species must be transported from the bulk of the gas to the oxide/gas interface
  - species must diffuse across (through) the oxide layer already present and get to the Si
  - then, the species chemically reacts at the Si interface to produce an oxide
- During the oxidation process, a portion of the Si wafer is consumed – and the resulting oxide expands upward during growth (relative to the original Si/air position)
- Si/SiO₂ interface moves into the silicon during the oxidation process.
- Densities & molecular weights of Si & SiO₂ used to show that growing an oxide of thickness \( x \) consumes a layer of silicon 0.44\( x \) thick.

Simple model/growth model:

Volume of one mole:
Molecular weight of Si/Density of Si → \( \text{Si} = \frac{M}{\rho_s} = \frac{28.09 \text{(g/mole)}}{2.33 \text{(g/cm³)}} = 12.06 \text{(cm³/mole)} \)

Molecular weight of SiO₂/Density of SiO₂ → \( \text{SiO}_2 = \frac{60.08 \text{(g/mole)}}{2.21 \text{(g/cm³)}} = 27.18 \text{(cm³/mole)} \)

Thickness of Si x Area/Thickness of SiO₂ x Area = Volume of 1 mol of Si/volume of 1 mol of SiO₂

\( \frac{\text{Vol}(\text{Si})}{\text{Vol}(\text{SiO}_2)} = 0.44 \)

Equation Format:

\[ N_s(AX_s) = N_{ox}(AX_{ox}) \]

\( X_s = \frac{N_{ox}}{N_s}X_{ox} = 0.44X_{ox} \)

- Utility – thin oxides (≤ 1000 Ang) use dry process (perform electrical device functions)
  - thick oxides (≥ 5000 Ang) use wet process – faster growth, lower quality, used for isolation
**Oxidation**

- Under a given oxidation condition
- oxide thickness grown on a (111)-substrate is larger than that grown on a (100)-substrate

Why?
- Because of the larger linear rate constant of the (111)-orientation.

**Note:**
- For a given temperature and time
- oxide film obtained using wet oxidation is about 5-10 times thicker than dry oxidation

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**Crystal Orientation – Wet Oxidation**

Oxide thickness vs. oxidation time for Si in H$_2$O at 640 Torr

Wet oxide growth at increased pressures

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Figure 11.8. Experimental results of silicon dioxide thickness as a function of reaction time and temperature for two substrate orientations. (a) Growth in dry oxygen. (b) Growth in steam.³
Oxide Growth vs. Temp & Pressure

Oxidation of P-doped Si in wet oxygen (95°C H₂O) as a function of temperature and concentration

Impurity Effects

P-type
Oxidation of B-doped Si in wet oxygen (95°C H₂O) as a function of temperature and concentration

N-type
Oxidation of P-doped Si in wet oxygen (95°C H₂O) as a function of temperature and concentration
Masking Properties of SiO$_2$

- Mask impurities during high temp diffusion
- Deep diffusions can take place in unprotected regions of Si, whereas no significant impurity penetration will occur in regions covered by SiO$_2$
- Arsenic & antimony diffuse slower than P
- Masking thicknesses of 0.5-1.0 µm are typical in IC processes
- Failure if 10% impurity fraction under mask as compared to background conc. in the Si
- Silicon nitride used to mask Ga

### Thickness of SiO$_2$ needed to mask B & P diffusions as a function of diffusion time at temperature

Selecting Oxidation

- Silicon nitride used as oxidation barrier
- Thin layer of SiO$_2$ oxide (10-20 nm) 1st grown to protect Si surface
- SiN deposited over surface & patterned using photolithography
- Oxidized – grows where not protected by SiN – semirecessed oxide structure (most common)
- Oxide growth occurs under edges causing nitride to bend up – bird’s beak
  - Lose geometry control in VLSI structures – must be minimized
- Fully recessed oxide formed by etching the Si prior to oxidation
  - Planar following SiN removal however subsequent processing reduces these advantages
Dielectric & Polysilicon Deposition

- Widely used in modern VLSI circuits
- Provide conducting regions, electrical insulation between metals, environmental protection
- Require uniform thickness & reproducible
- Most widely used material for film deposition (excluding metals)
  - Polycrystalline silicon – typically dope heavily n- or p-type
  - Silicon dioxide
  - Stoichiometric silicon nitride (Si₃N₄)
  - Plasma deposited silicon nitride
- Common deposition methods
  - Chemical vapor deposition (CVD)
  - Low pressure chemical vapor deposition (LPCVD)
  - Plasma enhanced chemical vapor deposition (PECVD)

Polycrystalline Si (Poly or polysilicon)

PolySi
- Pyrolyze silane (SiH₄) at 575-650°C (break apart silane)
- Conducting lines for multilevel metallization
- Contact for shallow junctions
- Usually deposited without dopants (but not always)
- Dopants (As, P, B) reduce ρ (resistivity) - added by diffusion or ion implantation

Silicon dioxide (CVD films)
- Dielectric insulator between conducting films
- Masks for diffusion and ion implantation
- Diffusion source – from doped oxides
- Capping doped films/Si – prevent dopant loss
- Gettering impurities – process which removes harmful impurities or defects
- Phosphorous-doped SiO₂ (P-glass) used as doping source
  - i.e. phosphosilicate glass or PSG
  - Inhibits diffusion of Na, softens & flows at 950-1100°C – creating a smooth topography — good for subsequent metal, enhances hydrophobicity
- Borophosphosilicate glass (BPSG) – flows at 850-950°C – over wafer surface like PR
Silicon Nitride

- Nearly impervious to moisture
- Si₃N₄ deposited at 700-900°C is used as an oxidation mask
- Plasma deposited silicon nitride (SiNH) forms at 200-350°C – used for passivation. The low T allows for deposition over Au or Al

CVD Techniques (most often used for deposition)
- Temp range 100-1000°C
- Pressure range 0.05 Torr – 760 Torr (1 atm)
- Reaction energy \(\rightarrow\) supplied by photons, glow discharge, thermal
- Poly & dielectric films have historically been deposited at 1 atm in a variety of reactor geometries
- Wafer(s) are placed on susceptor(s) heated by radiation using high intensity lamps, RF induction, or electrical resistance
- Horizontal reactors flow gas across the hot wafers, often at high velocity
- Vertical reactors often consist of a bell jar chamber with samples on a rotating assemble, perpendicular to gas flow

Plasma CVD

- Cylindrical reaction chamber made of quartz or stainless steel (with a view port)
- Capacitor (parallel plate) electrodes made of Al
- Samples lay on the bottom Al capacitor plate (or on a quartz plate placed on the Al plate)
- System is heated resistively (100-400°C)
- The source gas flows radially throughout the reaction chamber
- Used for SiO₂ & Si₃N₄
- Advantages
  - Low temperatures
  - Fast, easy
- Disadvantages
  - Limited capacity
  - Manual load/unload, gas purge, etc
  - Wafer contamination
CVD Reactors

Considerations in selecting a deposition process

- Substrate temperature
- Deposition rate
- Film uniformity
- Morphology
- Electrical properties
- Mechanical properties
- Chemical composition of dielectric films

Figure 11.9. Schematic diagrams of chemical-vapor deposition reactors. (a) Hot-wall, reduced-pressure reactor. (b) Parallel-plate plasma deposition reactor. *rf, radio frequency.

Silicon Dioxide

<table>
<thead>
<tr>
<th>TABLE 1 Properties of SiO2 Films</th>
</tr>
</thead>
<tbody>
<tr>
<td>Property</td>
</tr>
<tr>
<td>----------------------------------</td>
</tr>
<tr>
<td>Composition</td>
</tr>
<tr>
<td>Density (g/cm³)</td>
</tr>
<tr>
<td>Refractive index</td>
</tr>
<tr>
<td>Dielectric strength</td>
</tr>
<tr>
<td>End cap (A mm)</td>
</tr>
<tr>
<td>End cap (B mm) (abbreviation)</td>
</tr>
<tr>
<td>Step coverage</td>
</tr>
<tr>
<td>Products</td>
</tr>
</tbody>
</table>

Tetraethylorthosilicate (TEOS)

- Suitable for Polysilicon gates requiring a uniform insulating layer with good step coverage.

- For high-temp deposition (900°C)

\[ SiCl_4 + 2N_2O \xrightarrow{900°C} SiO_2 + 2N_2 + 2HCl \]

- Deposition gives excellent film uniformity & sometimes used to deposit insulating layers over polysilicon

NOTE: CVD SiO2 does not replace thermally grown oxides as best electrical properties are obtained from thermally grown films

Polysilicon Deposition

- Pyrolyze silane at 575-650°C in a low pressure reactor
  \[ SiH_4 \rightarrow Si + 2H_2 \]
- Two common low pressure deposition recipes
  - 100% silane at 25-130 Pa (0.2-1.0 Torr)
  - 20-30% silane in N_2 at 25-130 Pa
  - Deposition rates are 10-20 nm/min
- Deposition of polysilicon depends on temp, pressure, silane concentration, and dopant concentration
- Polysilicon may be oxidized
- Usually done in dry O_2, T=900-1000°C
- Polysilicon properties
  - Density = 2.3 g/cm³
  - Coefficient of thermal expansion - \( \alpha = 2 \times 10^{-6}/°C \)
  - Temp. coefficient of resistance – \( k = 1 \times 10^{-3}/°C \)
- Addition of oxygen to polysilicon increases the film resistivity
  \[ SiH_4 \rightarrow Si + 2H_2 \]
  \[ SiH_4 + xN_2O \rightarrow SiO_x + 2H_2 + xN_2 \]

Step Coverage

Conformal - Uniformity of the film thickness, regardless of topography, is due to the rapid migration of reactants after adsorption on the step surfaces

Non-conformal step coverage
- \( 0 \leq \theta_1 \leq 180° \) Top surface reactants come from many different angles
- \( 0 \leq \theta_2 \leq 90° \) Reactants arriving at the top of vertical wall
- \( \theta_1 \approx \tan^{-1}\left(\frac{W}{L}\right) \) Related to width of opening and distance from top

- Film thickness on the top surface is double that of a wall surface
- This type of step coverage is thin along the vertical walls, with a possible crack at the bottom of step caused by self-shadowing
- Most evaporated (or sputtered) materials have a nonconformal step coverage

Figure 11.12. Step coverage of deposited films.
(a) Conformal step coverage.
(b) Nonconformal step coverage.
**Silicon Nitride CVD**

$$3SiH_4 + 4NH_3 \xrightarrow{700-800^\circ C (1.4 atm)} Si_3N_4 + 12H_2$$  silane + ammonia

$$3SiCl_2H_2 + 4NH_3 \xrightarrow{700-800^\circ C (1.4 atm)} Si_3N_4 + 6HCl + 6H_2$$  dichlorosilane + ammonia

Good film uniformity and high wafer throughput

Refractive index \(\rightarrow\) related to composition

**Properties of silicon nitride**

<table>
<thead>
<tr>
<th>Property</th>
<th>LPCVD</th>
<th>Plasma</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature (^{\circ}C)</td>
<td>700-800</td>
<td>250-250</td>
</tr>
<tr>
<td>Composition SiN(_4)(H)</td>
<td>SiN(_4)H(_x)</td>
<td></td>
</tr>
<tr>
<td>Si/N ratio</td>
<td>0.75</td>
<td>0.8-1.2</td>
</tr>
<tr>
<td>Atom % H</td>
<td>4-8</td>
<td>20-25</td>
</tr>
<tr>
<td>Refractive index</td>
<td>2.01</td>
<td>1.8-2.5</td>
</tr>
<tr>
<td>Density (g/cm(^3))</td>
<td>2.9-3.1</td>
<td>2.4-2.8</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>6-7</td>
<td>8-9</td>
</tr>
<tr>
<td>Resistivity (ohm-cm)</td>
<td>10(^{10})</td>
<td>(10^8-10^{13})</td>
</tr>
<tr>
<td>Dielectric strength (10^9 V/m)</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>Energy gap (eV)</td>
<td>5</td>
<td>4-5</td>
</tr>
<tr>
<td>Stress ((10^9 \text{dyne/cm}^2))</td>
<td>10 T</td>
<td>2-5 T</td>
</tr>
</tbody>
</table>

**SiN Plasma CVD**

- \(\text{Si}_3\text{N}_4\)
- High tensile stress \(\sim 1E10 \text{dyne/cm}^2\)
- \(1 \text{Pa} = 1\text{N/m}^2 = 1E-5 \text{bar} = 10 \text{dyne/cm}^2 = 7.501E-3 \text{torr}\)
- Films \(d > 200 \text{nm}\) sometimes crack due to the high stress

SiN Plasma CVD (usually radial flow, parallel plate, hot wall reactor)

\[SiH_4 + NH_3 \rightarrow SiNH + 3H_2\]  Argon plasma

\[2SiH_4 + N_2 \rightarrow 2SiNH + 3H_2\]  Reduce silane in a nitrogen discharge

The products depend strongly on the deposition conditions
- Plasma deposited films contain large H concentrations

**Other materials**
- Silicon oxy nitride (SiON)
- Al oxide, Al nitride, Ti oxide \(\text{high } \rho, \varepsilon\)
- Polymides – spin and cure \((300-350^\circ C) \rightarrow \text{planar surfaces, poor thermal stability and moisture protection}\)
**MicroElectroMechanical Systems (MEMS)**

**Metallization**

- Desired properties of the metallization for ICs, MEMS, & microelectronics
- Low resistivity
- Easy to form
- Easy to etch for pattern generation
- Should be stable in oxidizing ambients
- Mechanical stability; good adherence, low stress
- Surface smoothness
- Stability throughout processing, including high temp sinter, dry or wet oxidation, gettering, phosphorus glass (or any other material) passivation, metallization
- No reaction with final metal, aluminum
- Should not contaminate devices, wafers, or working apparatus
- Good device characteristics and lifetimes
- For window contacts – low contact resistance, minimal junction penetration, low electromigration
- Silicide – interface formed between Si & metal
Physical Vapor Deposition

- Most common methods
  - Evaporation – source material heated above melting point in evacuated chamber, evaporated atoms travel at high velocity in straight line trajectories. Heated by resistive, RF, or focus electron beam
  - E-beam evaporation
  - Plasma spray deposition
  - Sputtering – a source of ions is accelerated toward the target and impinged on its surface.
- Ti, Al, Cu, TiN, Au can be deposited this way

![Figure 11.18](image)

(a) Standard sputtering, (b) long-through sputtering, and (c) sputtering with a collimator.


Metal CVD Deposition

- CVD metallization offers
  - Conformal coating
  - Good step coverage
  - Coat a large # of wafers simultaneously
- Basic CVD setup is the same as the deposition of dielectrics and polysilicon

A schematic drawing of a multilevel metallization structure

Four types of CVD systems (a) APCVD, (b) hot-wall LPCVD using three zone furnace tube, (c) Parallel-pole plasma-enhanced, (d) PECVD

CVD of Metals

- Process by which a metal film is deposited by a chemical reaction or pyrolytic decomposition in the gas phase, in the neighborhood of the substrate
- Advantages
  - Conformal metal films (good step coverage)
  - Large # of wafers/run
  - Lower resistivity than with physical evaporation
  - Refractory metals
  - Useful for depositing heavy metals (i.e. W)

Chemistry (Tungsten) W

\[
WF_6 \xrightarrow{\text{pyrolysis}} W + 3F_2 \\
WF_6 + 3H_2 \xrightarrow{\text{reduction at 600-900°C}} W + 6HF
\]

HF – very toxic, will “eat” your car’s windows

Other metals – Mo, Ta, Ti can be deposited by hydrogen reduction in an LPCVD reactor

\[
2MCl_3 + 5H_2 \xrightarrow{600-800°C} 2M + 10HCl
\]

Al deposition using an MO source – tri-isobutyl aluminum (MO = metalorganic)

\[
2[(CH_3)_2CHCH_2]_3Al \rightarrow 2Al + 3H_2 + \text{by products}
\]

Deposition by Evaporation

- Thermal (resistive heating)
- Electron beam (e-beam)

Potential disadvantages
- Source filament/crucible contamination
- Ionizing x-rays penetrate substrate, damage lattice

An evaporation source using electron-beam heating. The beam is generated out of the line of sight of the source and is focused into it by a B-field. A heated filament supplies electrons, and the accelerating electrodes form them into a beam.
Factors governing step coverage in evaporation

(a) Perpendicular step on perpendicular substrate. No coverage

(b) Rotating planetaries with some substrate inclination. Improved coverage

(c) Same configuration with substrate heating. Further improvement

(d) Reduced slope of step, plus rotation and heating. No thinning over step

Sputtering

- Sputter depositions has a threshold energy – this energy (of bombarding ions) must be exceeded before sputtering begins
- Thresholds
  - 10 eV for Al
  - 15 eV for Pd
  - 21 eV for Mo
  - 34 eV for Pt
  - Up to ~100 eV for others

"sputter yield" $\equiv \frac{\# \text{ atoms liberated from target}}{\# \text{ of incident ions}} = \gamma$

- Typically want operation with sputter yield $\geq 1.0$

\[ N = \left( \frac{J}{qZ} \right)^{\gamma} \]

$N \equiv$ flux or # of atoms per unit area per unit time leaving the target

$J \equiv$ current density of the bombarding ion

$Z \equiv$ # of charges per ion
Lithography

- Transfer geometric patterns on a mask to a thin layer of radiation sensitive material (called resist) covering the surface of a semiconductor wafer.
- Transfer stored geometric patterns (in a computer memory) to a thin resist layer as above (direct write)
  - Optical lithography
  - Electron beam lithography
  - X-ray lithography
  - Ion Beam lithography
- Optical lithography
  - Ultraviolet radiation
  - (λ ~ 0.2 to 0.4 µm)
  - Resist ⇒ photoresist

Exposure Tool performance (3 parameters)
- Resolution – minimum feature dimension that can be transferred with high fidelity to a resist film
- Registration – measure of how accurately patterns on successive masks can be aligned
- Throughput – number of wafers that can be exposed per hour for a given mask level
Exposure Methods

- Proximity – shadow printing method used to minimize mask damage
- Minimum linewidth or critical dimension \( CD = \frac{\lambda}{2g} \) (gap between mask/wafer & includes resist thickness)

Schematic of optical shadow printing techniques: (a) contact printing, (b) proximity printing.

**Contact printing**
- In physical contact
- Approximately 1 µm resolution
- Major drawback – dust particles/Si dust
- Can be imbedded in mask
- Permanently damaged

**Proximity printing**
- Small gap → 10-50 µm
- Gap results in optical diffraction
- Approximately 2-5 µm resolution

Image partitioning techniques for projection printing: (a) annual-field wafer scan, (b) 1:1 step-and-repeat, (c) M:1 reduction step-and-repeat, and (d) M:1 reduction step-and-scan.
Projection Printing

Projection Printing
- Avoids the mask damage problem of shadow & contact printing
- Projects image of the mask pattern onto resist-coated wafer
- Many centimeters between mask & wafer
- To increase resolution – only small portion of mask exposed at a time
- Image scanned or stepped across entire wafer
- Resolution of projection system (~ 1 – 0.07 µm) can be calculated by

\[ l_n = k_1 \frac{\lambda}{NA} \]  \hspace{1cm} (2)
\[ k_1 = \text{process dependent factor} \]
\[ \lambda = \text{exposure wavelength} \]
\[ NA = \text{numerical aperture} \]

\[ NA = \frac{\lambda}{2} \tan(\frac{\theta}{2}) \]  \hspace{1cm} (3)

where \( \theta \) = half-angle of the cone of light converging to a point image at the wafer

Degrees of Freedom (DOF)

\[ DOF = \frac{\pm l_n / 2}{\tan \theta} = \frac{\pm l_n / 2}{\sin \theta} = k_2 \frac{\lambda}{(NA)^2} \]  \hspace{1cm} (4)

\[ k_2 = \text{process dependent factor} \]

Lithography Masks

- Used in IC manufacturing
- Use CAD design system to completely describe circuit patterns electrically
- Masks consists of fused silica substrate covered with a chromium layer

Figure 12.7. An integrated-circuit photomask.¹

Mask plates – increasing cost & performance
- Low cost glass – emulsion - $100 set
- Quartz, BSG – emulsion, chrome, iron oxide, several thousand $ for set
- Sapphire – $10’s of thousand – chrome,
Exposure Defects/Yield

- Patterns on a mask represent one level of a design
- Typically – 15-20 different masks levels required for a complete IC process cycle
- Standard size mask 15 x 15 cm
- 0.6 cm thick
- Defect density – mask defects
  - Introduced during the manufacture of the mask
  - During subsequent litho processes
- Yield – defined as the ratio of good chips/wafer to the total # of chips/wafer
- Increase yield through
  - inspection
  - Cleaning of masks
  - ultraclean processing area

\[ Y \cong e^{-DA} \]
\[ D = \text{average # of fatal defects/unit area} \]
\[ A = \text{area of an IC chip} \]
\[ N = \# \text{ of levels} \]

Figure 12.8. Yield for a 10-mask lithographic process with various defect densities per level.

Clean Room

- Integrated circuit fabrication requires a clean processing room
- Dust and other particulates can settle on masks and/or device layers ⇒ causes defects & circuit failure
- Class 100 & below ⇒ workers wear body suits & headgear w/ respirator

Figure 12.2. Particle-size distribution curve for English (---) and metric (—) classes of cleanrooms.4
- Temp and humidity must be tightly controlled
- Tighter control is necessary for cleanroom environment when minimum feature lengths of devices are reduced to the deep submicron range
- Most IC fab rooms require at least a Class 100 cleanroom
  - i.e. dust count ~ 4 orders of magnitude lower than ordinary room air
  - In litho area, a class 10 or lower is necessary

### Clean Room Requirements

<table>
<thead>
<tr>
<th>Class</th>
<th>Number of 0.5-μm particles per ft³ (m³)</th>
<th>Number of 5-μm particles per ft³ (m³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10,000</td>
<td>10,000 (250,000)</td>
<td>65 (23,500)</td>
</tr>
<tr>
<td>1,000</td>
<td>1,000 (25,000)</td>
<td>6.5 (2,300)</td>
</tr>
<tr>
<td>100</td>
<td>100 (2,500)</td>
<td>0.65 (220)</td>
</tr>
<tr>
<td>10</td>
<td>10 (250)</td>
<td>0.005 (22)</td>
</tr>
<tr>
<td>1</td>
<td>1 (35)</td>
<td>0.0005 (2.2)</td>
</tr>
</tbody>
</table>

*It is very difficult to measure particle counts below 10 per ft³.*

---

**AFIT Cleanroom**

---

**MicroElectroMechanical Systems (MEMS) EE 480/680, Summer 2006, WSU, L. Starman**
Photoresist

- Radiation sensitive compound
- Classified as either positive or negative

**Positive**
- Exposed regions become more soluble and remove easily in development process
- Patterns formed (images) are the same as those of the mask

**Negative**
- Exposed regions less soluble
- Patterns formed are the reverse of the mask patterns

- Positive photoresists made up of three components
  - Photosensitive compound – prior to exposure, insoluble in developer solution. After exposure, absorbs radiation & changes chemical structure and become soluble & removable during development
  - Base resin
  - Organic solvent – keeps the resist a fluid/liquid for ease of application

- Negative resists are polymers combined with a photosensitive compound
  - After exposure, absorbs the optical energy and converts it into chemical energy to initiate a polymer linking reaction.
  - Causes crosslinking of polymer molecules which ends up having a higher molecular weight and becomes insoluble in developer solution.

- Major drawback – during development process, whole resist mask swells by absorbing developer solvent. This swelling limits the resolution of negative resist.

- Typical exposure energies for a 1 µm-thick negative resist coating are 10-20 mJ/cm²
- Negative resist solvents are usually mixtures of hydrocarbons

---

**Contrast ratio:**

Positive resist:

\[
\gamma = \left[ \ln\left( \frac{E_R}{E_i} \right) \right]^{-1}
\]

\(E_T\) corresponds to the sensitivity
\(E_i\) is the energy obtained by drawing the tangent at \(E_T\) to reach 100% resist thickness

- Sensitivity is defined as the energy required to produce complete solubility in the exposed region

- A larger \(\gamma\) implies a higher solubility of the resist with an incremental increase of exposure energy & results in sharper images

Negative resist:

\[
\gamma = \left[ \ln\left( \frac{E_i}{E_T} \right) \right]^{-1}
\]
MicroElectroMechanical Systems (MEMS)

Exposure vs Developer

A typical set of curves showing development speed versus exposure energy for positive resist in a function of concentration of the developer. (Figures courtesy of and reprinted by permission of, Total Corporation, all rights reserved.)

Resist Thickness

\[ Z = \frac{kP^2}{\sqrt{W}} \]

where

- \( Z \) = resist thickness (µm)
- \( P \) = % of solids in the resist
- \( V \) = viscosity (thickness) of resist
- \( W \) = rotational velocity of the spinner
- \( k \) = empirical constant, \( \mu \text{m} - \sqrt{\text{sec}} \)

- Typically want 1.0 – 1.5 µm thick
Silicon Wafer Cleaning Procedure

Generally not performed in this fashion
- **Typical Method**
  - Acetone spin 30 sec
  - Methanol spin 30 sec
  - Isopropyl spin 20 sec
  - DI water spin 20 sec
  - If Si, dip in BOE for 15 sec
    - Removes native oxides
  - DI rinse for 60 + sec
  - Dry with $N_2$

Pattern Transfer

- Cleanroom illuminated with yellow light
  - Why? Photoresists are not sensitive to wavelengths greater than 0.5 µm
- Following cleaning and hotplate bake
- Wafer placed on vacuum spindle
- Liquid photoresist is applied to center of wafer
- Wafer rapidly accelerated up to a constant rotational speed
- Maintained at this speed for ~ 30 sec
- Spin speed generally ranges from 1000-10,000 rpm to coat uniformly
- Resist film thickness about 0.5-1.0 µm
- Resist thickness correlated to its viscosity
- Following spin, wafer placed on hotplate for soft bake (typically 90°-180°C for 60-120 seconds)
- Bake used to remove solvents & increase adhesion
- Align wafer with mask and expose to UV
- Develop resist and presto, you have your design pattern
  - If not, you need remedial training and start over
- Rinse off developer ~60 sec in DI water & dry with $N_2$
- Continue with deposition/etch processes
- **NOTE:** each PR will have its own spin speed & developer times and settings

![Figure 12.10. Details of the optical lithographic pattern transfer process.](image-url)
Figure 12.11. Liftoff process for pattern transfer.

Factors affecting alignment accuracy.
(a) step-and-repeat error; linear spacing. (b) step-and-repeat error; reticle rotation. (c) Run-in/run-out of mask relative to substrate. (d) Alignment error: translational. (e) Alignment error: rotational.
Next Generation Litho Methods

- Optical lithography – widely used due to:
  - High throughput
  - Good resolution
  - Low cost
  - Ease in operation
  - However, limited in deep-submicron IC processes
- Need postoptical lithography to process deep-submicron or even nanometer ICs
- New techniques
  - Electron beam
    - Primarily used to make photomasks
  - X-ray
    - Candidate to replace optical lithography, can be used for the fabrication of IC’s at 100 nm
  - Ion Beam
    - Can achieve the highest resolution, used to repair the masks for optical lithography

Electron Beam Lithography

- Electron gun – generates the beam of electrons
- Tungsten thermionic-emission cathode used for electron gun
- Condenser lenses used to focus the electron beam to a spot size 10-25 nm in diameter
- Beam blanking plates turn the electron beam on and off
- Precision mechanical stage used to position the substrate to be patterned
- Advantages
  - Permits generation of submicron resist geometries
  - Highly automated
  - Precisely controlled operation
  - Greater depth of focus
  - Direct patterning on a wafer without using a mask
- Disadvantages
  - Have low throughput ~10 wafers/hr at less that 0.25 µm resolution
  - Fine for mask making
Scan Techniques

(a) Raster scan writing scheme; (b) vector scan writing schemes; and (c) shapes of electron beam: round, variable, cell projection.

- Raster scan
  - Resist patterns are written by a beam that moves through a regular mode, vertically oriented
  - Beam scans sequentially over every possible location on the mask and is blanked (turned off) where no exposure is required
  - Pattern must be subdivided into individual addresses
  - Pattern must have a minimum incremental interval evenly divisible by beam address size

- Vector scan
  - Beam directed only to the requested pattern features and jumps from feature to feature rather than scanning the whole chip
  - Average exposed region is only 20% of the chip area – saves time

Electron Resist

- Electron resists are polymers
  - Exposure causes chemical bonds to be broken – molecular weight is reduced which enhances dissolving in developer solution
  - Common positive resists – PMMA & PBS (poly-butene-1 sulfone)
  - Achieve resolution of 0.1 µm or better

- Negative resist
  - Causes radiation-induced polymer linking
  - Higher molecular weight
  - Common negative resist – poly-glycidyl methacrylate-co-ethyl acrylate (COP)
  - Swells during development – resolution limited to ~ 1 µm

PMMA – polymethyl methacrylate (PMMA)
**X-Ray Lithography**

- Uses a shadow printing method similar to optical proximity printing
- X-ray wavelength is about 1 nm, and printing is through a 1X mask in close proximity (10-40 µm) to the wafer
- X-rays produced in vacuum and in He environment separated by a thin vacuum window (usually beryllium)
- Mask substrate will absorb 25%-35% on the

![X-Ray Lithography Diagram]

**Ion Beam Lithography**

- Higher resolution than optical, e-beam, or x-ray lithography
- Higher ion mass ⇒ less scatter
- Use PMMA resist (more sensitive to ions that to e’s)
- Scanning focused beam or masked beam system
- Ion optics for scanning systems – more difficult to operate than electron optic scanning systems
- Ion source: ionize gas surrounding a W-tip liquid metal flowing to W-tip. Ion current density
  - Ga+ 0.1 µm spot ⇒ 1.5 A/cm²
  - H+ 0.65 µm spot ⇒ 15 A/cm²
- Must use electrostatic
- (rather than magnetic) “lenses”

![Ion Beam Lithography Diagram]
Etching

- Two types of etching
  - Wet chemical etching
  - Dry plasma etching

**Wet etching**
- Transfer pattern from a resist to a film on a substrate (oxide, epilayer) – or directly to the substrate
- Proceeds at a relatively slow, controlled rate. Relies on reproducible etch rates with human monitoring
- Etch rates tend to be limited by the rate of diffusion of the reactant through a stagnant layer that covers the surface
- Wet etches are often limited by the rate of dissolution of the reaction products into the solution.
- Agitation of the solution helps to increase the etch rate by enhancing this out diffusion
- The etching of poly and amorphous materials is isotropic
- Wet etching of crystalline materials may be isotropic or anisotropic – depending on the nature of the reaction kinetics
- Isotropic etches => polishing etches, result in smooth surfaces
- Used for lapping and polishing to give an optically flat, damage-free surface.

Wet Etching

- Mechanisms for wet chemical etching involve three essential steps
- Reactants are transported by diffusion to the reacting surface
- Chemical reactions occur at the surface
- Products from the surface removed by diffusion
- Both agitation & temperature of the etchant solution will influence the etch rate
- Etching performed by immersion (requires agitation to ensure etch uniformity and consistent etch rate) or spraying the wafers with the etchant solution
- Spray etching replacing immersion etching
  - Increases the etch rate
  - Increases uniformity by constant fresh supply of etchant to wafer

- Etch rate uniformity given by:
  \[
  \text{Etch rate uniformity} \, (\%) = \frac{(\text{maximum etch rate} - \text{minimum etch rate})}{\text{maximum etch rate} + \text{minimum etch rate}} \times 100\%
  \]

![Figure 12.21. Basic mechanisms in wet chemical etching](image)
**Oxide Etching**

- Buffered oxide etch – commonly used to etch windows in silicon dioxide layers.
- BOE contains HF and a buffer in water
- Room temp (~25°C), BOE etches SiO2 film much more rapidly than Si or PR
- Depending on the density of the SiO2 film, etch rate \( r \approx 10 \text{ to } 100 \text{ nm/min at RT} \)
- A high concentration of phosphorous in the oxide enhances the etch rate. A reduced etch rate occurs when a high concentration of boron is present (PSG, BSG)
- Length of etch may be controlled visually by monitoring test wafers
- Hydrophobic condition ("beading") indicates completion \( \Rightarrow \) HF & H2O wet silicon dioxide (hydrophilic) but not silicon

\[
\text{SiO}_2 + 4\text{HF} \rightarrow \text{SiF}_4 + 2\text{H}_2\text{O}
\]

Buffer HF with ammonium fluoride (NH4F)

\[
\text{NH}_4\text{F} \rightarrow \text{F}^- + \text{NH}_4^+
\]

**Insulator-Conductor Etchants**

<table>
<thead>
<tr>
<th>Material</th>
<th>Etchant Composition</th>
<th>Etch Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO2</td>
<td>28 ml HF, 170 ml H2O</td>
<td>Buffered HF, 1000 Å/min</td>
</tr>
<tr>
<td></td>
<td>113 g NH4F</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15 ml HF, 10 ml HNO3</td>
<td>120 Å/min</td>
</tr>
<tr>
<td></td>
<td>300 ml H2O</td>
<td></td>
</tr>
<tr>
<td>Si3N4</td>
<td>Buffered HF</td>
<td>5 Å/min</td>
</tr>
<tr>
<td></td>
<td>H3PO4</td>
<td>100 Å/min</td>
</tr>
<tr>
<td>Al</td>
<td>1 ml HNO3, 4 ml CH3COOH, 4 ml H3PO4, 1 ml H2O</td>
<td>350 Å/min</td>
</tr>
<tr>
<td>Au</td>
<td>4 g KI, 1.5 ml H2O</td>
<td>1 μm/min</td>
</tr>
<tr>
<td>Mo</td>
<td>5 ml H3PO4, 4 ml CH3COOH</td>
<td>0.5 μm/min</td>
</tr>
<tr>
<td></td>
<td>2 ml HNO3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>130 ml H2O</td>
<td></td>
</tr>
<tr>
<td>Pt</td>
<td>1 ml HNO3, 7 ml HCl</td>
<td>300 Å/min</td>
</tr>
<tr>
<td>W</td>
<td>34 g KCl, 34 g KOH, 13.4 g K,F,Fe(NO3)4, H2O to make 1 liter</td>
<td>1000 Å/min</td>
</tr>
</tbody>
</table>
### Etch Rates

- Rate determining step (slowest reaction step)
- Rule of thumb: reaction rates double with every 10°C of increased temperature
- Thus ±1°C can change etch rates ~10%, and temperature control is important in etching reactions
- Etching of crystalline silicon
- Wet etching proceeds by oxidation, followed by the dissolution of the oxide by a chemical reaction
- Common etchants for silicon

\[
\text{HNO}_3 \text{ (nitric acid)} + \text{HF (hydrofluoric acid)} \text{ in } \text{H}_2\text{O} \text{ or } \text{CH}_3\text{COOH (acetic acid)}
\]

\[
\text{Si} + 2\text{H}^+ \rightarrow \text{Si}^{2+} \quad \text{(auto catalytic process) higher oxidation state}
\]

\[
\text{Oxidizing specie (OH)}^- \text{ formed by the dissociation of } \text{H}_2\text{O}
\]

\[
\begin{align*}
\text{Si}^{2+} + 2\text{OH}^- & \rightarrow \text{Si(OH)}_2 \rightarrow \text{SiO}_2 + \text{H}_2 \\
& \text{liberates } \text{H}_2
\end{align*}
\]

The HF is used to dissolve \(\text{SiO}_2\)

\[
\text{SiO}_2 + 6\text{HF} \rightarrow \text{H}_2\text{SiF}_6 + 2\text{H}_2\text{O}
\]

Takes place in MEMS process to remove \(\text{SiO}_2\)

<table>
<thead>
<tr>
<th>Etchant</th>
<th>Etchant</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\text{SiO}_2)</td>
<td>25 ml HF</td>
<td>(\text{BH}_{4}), 100-500 Å/min at 25°C</td>
</tr>
<tr>
<td></td>
<td>170 ml HNO(_3)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15 ml (\text{H}_3\text{PO}_4)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 ml (\text{H}_2\text{SO}_4)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 ml (\text{H}_2\text{O})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 ml (\text{HF})</td>
<td>100 Å/min</td>
</tr>
<tr>
<td>(\text{YSG})</td>
<td>7 ml HF</td>
<td>(\text{NH}_3), 300 Å/min for 9 months (\text{Si}), 50 Å/min for (\text{SiO}_2)</td>
</tr>
<tr>
<td></td>
<td>190 ml (\text{HNO}_3)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>100 ml (\text{H}_2\text{O})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>60 ml (\text{H}_2\text{O})</td>
<td>100 Å/min</td>
</tr>
<tr>
<td>(\text{PSG})</td>
<td>25 ml HF</td>
<td>(\text{BH}_{4}), 5000 Å/min for 9 months (\text{Si})</td>
</tr>
<tr>
<td></td>
<td>170 ml (\text{HNO}_3)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>130 ml (\text{H}_2\text{O})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 ml (\text{H}_2\text{SO}_4)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 ml (\text{H}_2\text{O})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 ml (\text{HF})</td>
<td>100 Å/min</td>
</tr>
<tr>
<td>(\text{SiN}_x)</td>
<td>30 ml HF</td>
<td>(\text{SiO}_2), 100 Å/min at 80°C</td>
</tr>
<tr>
<td></td>
<td>170 ml (\text{HNO}_3)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>50 ml (\text{H}_2\text{O})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 ml (\text{H}_2\text{SO}_4)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5 ml (\text{HF})</td>
<td>100 Å/min at 80°C</td>
</tr>
<tr>
<td>Poly-silicon</td>
<td>5 ml HF</td>
<td>100 Å/min, smooth edges</td>
</tr>
<tr>
<td></td>
<td>100 ml (\text{HNO}_3)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>80 ml (\text{H}_2\text{O})</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 ml (\text{HF})</td>
<td>1500 Å/min</td>
</tr>
<tr>
<td>(\text{SiPOS})</td>
<td>1 ml HF</td>
<td>2000 Å/min for 20% (\text{O}_2) film</td>
</tr>
<tr>
<td></td>
<td>10 ml (\text{HNO}_3)</td>
<td></td>
</tr>
</tbody>
</table>
Orientation-dependent etching. (a) Through window patterns on <100>-oriented silicon; (b) through window patterns on <110>-oriented silicon.

KOH in water & isopropanol

<table>
<thead>
<tr>
<th>(100)</th>
<th>0.6 μm/min</th>
<th>@ T=80°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>(110)</td>
<td>0.1 μm/min</td>
<td></td>
</tr>
<tr>
<td>(111)</td>
<td>0.006 μm/min</td>
<td></td>
</tr>
</tbody>
</table>

Ratio of etch rates 100:16:1

The width of the bottom surface is given by

\[ W_b = W_o - 2/l \cot 54.7^\circ \]
\[ W_e = W_o - \sqrt{2}l \]

where \( W_o \) = width of the window on wafer surface
\( \omega \) = the etched depth

**Etch Compositions - Rates**

<table>
<thead>
<tr>
<th>Material</th>
<th>Buffer</th>
<th>Recipe</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Au</td>
<td>HCl</td>
<td>1 ml</td>
<td>80°C, free etch, can be used with palladium as etchant.</td>
</tr>
<tr>
<td></td>
<td>H2O</td>
<td>2 ml</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HNO3</td>
<td>4 ml</td>
<td>1 ml HNO3, 1 ml HF, 1 ml HClO4, 1 ml H2O.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6%–4% H2O, &gt;30 A/min, no etch.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.1 M Na2Si03, 0.1 M KOH, 0.1 M K2SO4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000–2000 Å/min, no etch.</td>
</tr>
<tr>
<td>Ar</td>
<td>HNO3</td>
<td>1 ml</td>
<td>25–30 Å/min, approx. 600 Å/min.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 ml</td>
<td>0.5–1.5 μm, can be used with resist.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40 ml</td>
<td>H2O.</td>
</tr>
<tr>
<td>Ag</td>
<td>HNO3</td>
<td>1 ml</td>
<td>500–600 Å/min, can be used with resist, must be cleaned rapidly after etching.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ml H2O</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>80 ml</td>
<td>H2O.</td>
</tr>
<tr>
<td>Cr</td>
<td>H2SO4</td>
<td>1 ml</td>
<td>100 Å/min, rough etch.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ml HCl</td>
<td>100 Å/min, rough etch.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ml H2O</td>
<td>100 Å/min, rough etch.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ml 30% H2O2</td>
<td>100 Å/min, rough etch.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ml H2O2</td>
<td>solution</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 ml H2SO4</td>
<td>250–1000 Å/min, no etch, resist mask can be used.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 ml H2O</td>
<td>1000 Å/min, etch at 80°C.</td>
</tr>
</tbody>
</table>

| Cu       | H2SO4  | 1 ml   | 1000 Å/min, rough etch. |
|          |        | 1 ml HCl | 1000 Å/min, rough etch. |
|          |        | 1 ml H2O2 | 1000 Å/min, rough etch. |
|          |        | 1 ml H2O | 1000 Å/min, rough etch. |
|          |        | 10 ml H2O2 | 1000 Å/min, rough etch. |
**Comparison of wet chemical etching and dry etching for pattern transfer.**

**Etch Techniques - Methods**

**Dry Etching Summation**

- Major disadvantage of wet chemical etching for pattern transfer is the undercutting of the layer under the mask, results in loss of resolution in etched pattern.
- In practice, for isotropic etching, the film thickness should be about one-third or less of the resolution required.
- If patterns are required for resolutions much smaller than the film thickness, anisotropic etching must be used.
- Dry etching techniques include:
  - Plasma etching
    - fully or partially ionized gas composed of equal #s of positive & negative charges & a different # of unionized molecules
    - Produced when an E-field of sufficient magnitude is applied to a gas, causing the gas to break down & become ionized
  - Reactive ion etching (RIE)
    - Extensively used in microelectronic industry
    - Uses parallel-plate diode system, RF capacitive-coupled bottom electrode which holds the wafer.
    - Low etch selectivity when compared to traditional barrel etch systems
  - Sputter etching
  - High density plasma (HDP) etching
Impurity Overview

- Basic diffusion process
  - under high temp & high concentration-gradient conditions
- Extrinsic diffusion
  - impurity profiles for constant diffusivity & concentration-dependent diffusivity
- Diffusion related processes
  - impact of lateral diffusion
- Range of implanted ions
  - process & advantages
- Implant damage & annealing
  - ion distribution in crystal lattice & how to remove lattice damage
- Implant related processes
  - masking, high-energy implantation, and high current implantation

Diffusion Doping

- Diffusion (and ion implantation) provides an important means of introducing controlled amounts of chemical impurities (dopants) into the lattice of a crystalline semiconductor substrate
- Diffusion is used for pn junctions, bipolar transistors, n-tubs for CMOS, selectively disordering regions of lasers, ohmic contact formation, et al.
- In practice, semiconductor wafers are placed in a furnace and an inert gas (N₂) that contains the desired dopant is passed over the wafers. In addition to gaseous dopant sources, liquid and solid sources are used
- Diffusion
  - slowly & high temp
- Ion implant
  - Gaussian distribution func.
  - Fast & at room temp
  - Peak – dependent on incident ion energy
  - Anneal ions to activate them

Comparison of (a) diffusion and (b) ion-implantation techniques for the selective introduction of dopants into the semiconductor substrate.
Diffusion System

Diffusions in Si - the furnace & gas flow arrangements are similar to those used in oxidation systems.

Diffusions in GaAs are done in sealed ampules containing an As overpressure or open-tube furnace with a doped oxide capping layer (SiN). Overpressure to prevent the loss of As by decomposition or evaporation.

Chemical reaction for phosphorus diffusion using liquid source:

\[ 4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \]

P₂O₅ forms a glass on Silicon wafer & then reduced to P by Silicon.

Silicon Diffusion Implementation

- 800-1200°C
- P-type (B)
  - BN - boron nitride (solid)
  - BBr₃ - boron bromide (liquid)
  - B₃H₆ - diborane (gas)
- N-type (As/P)
  - As₂O₃ - arsenic trioxide (solid)
  - P₂O₅ - phosphorous pentoxide (solid)
  - AsCl₃ - arsenic trichloride
  - POCl₃ - phosphorous oxychloride
  - AsH₃ - arsine
  - PH₃ - phosphine
- All dopants have solid solubilities
  - > 5E20 cm⁻³ at the temperatures of interest
Mechanisms of Diffusion and Doping

- Diffusion describes the process by which atoms move in a crystal lattice
- Although this includes self-diffusion, our primary interest is the diffusion of impurity atoms that are introduced into the lattice for the purpose of altering its electronic properties
- Concentration gradients, temperature, geometrical features (orientation, defect densities), and bonding strengths play an important role in the diffusion process
- The wandering of impurities in a lattice takes place by a series of “random” jumps in three dimensions
- A flux of diffusing species results if there is a concentration gradient
- Interstitial Diffusion
- Substitutional Diffusion
- Interchange Diffusion
- Combination Effects
- Diffusion is fast if some defects are present in the crystal
Impurity Doping Mechanisms

• Vacancy or substitutional
  – Impurity atoms wander through the crystal by jumping from one lattice site to the next, substituting for the original host atom. It is necessary that this adjacent site be vacant.
  – vacancies must be present to allow substitutional diffusion to occur.
  – Will not occur in a perfect crystal.

• Interstitial Diffusion
  – Impurity atoms move through the crystal by jumping from one interstitial site to the next. They may start at either lattice or interstitial sites and may end up in either type of site.
  – Interstitial diffusion requires that their jump motion occur from one interstitial site to another adjacent interstitial site.
  – Can occur in a perfect crystal.

• Dissociative Mechanism
  – Substitutional atom can become an interstitial (occupy both sites).
  – This mechanism may control diffusion.
    • Cu, Ni, Au in Si
    • Zn, Cd, Cu in GaAs.

• Interchange diffusion
  – Two or more atoms diffuse by an interchange process.
  – Direct interchange involves two atoms and a cooperative interchange involves a large number of atoms.
  – The probability of interchange diffusion is relatively low.

• Combination Effects
  – As name implies, a fraction of the impurity atoms may diffuse substitutionally and the rest interstitially (two stream process).
  – Some diffusion atoms may end up in substitutional sites, others in interstitial sites.

Ion Implantation

• A useful alternative to high temperature diffusion for doping (target wafer held at low temp).
• Impurity gas (BF₃, AsH₃, O₂, etc.) is ionized via a high voltage accelerator.
• Beam of ionized impurity atoms (plus molecular fragments) with ~1 cm diameter is generated.
• Beam current is ~10 µA to 1 mA, giving a charge Q transported down a “linear accelerator”.
• Implant dose range 10¹² to 10¹⁸ atoms/cm².
• Good for making small devices.
• Typical ion energies 30 to 300 KeV – up to ~1 MeV.
• Average depths ranging from 10 nm to 10 µm.
• Advantages: precise control and reproducibility of impurity dopings and its lower processing temperature.
Ion Implantation

Nature of the Concentration Profile

Due to Ion Implantation

<table>
<thead>
<tr>
<th>Distance from Mean Value</th>
<th>Magnitude of Ion Concentration (Normalized to Peak Value)</th>
</tr>
</thead>
<tbody>
<tr>
<td>γ</td>
<td>1</td>
</tr>
<tr>
<td>1.18γR_p</td>
<td>0.5</td>
</tr>
<tr>
<td>2.14γR_p</td>
<td>10^-1</td>
</tr>
<tr>
<td>3.04γR_p</td>
<td>10^-2</td>
</tr>
<tr>
<td>3.72γR_p</td>
<td>10^-3</td>
</tr>
<tr>
<td>4.29γR_p</td>
<td>10^-4</td>
</tr>
<tr>
<td>4.81γR_p</td>
<td>10^-5</td>
</tr>
<tr>
<td>5.57γR_p</td>
<td>10^-6</td>
</tr>
<tr>
<td>5.87γR_p</td>
<td>10^-7</td>
</tr>
</tbody>
</table>

(a) implant through an amorphous oxide layer, (b) misorient the beam direction to all crystal axes, and (c) predamage on the crystal surface.

Model for a diamond structure, viewed along a <110> axis.

Ion Stopping

Two stopping mechanisms

• Nuclear stopping – transferring energy to the target nuclei
  \[ S_n(E) = \frac{dE}{dx} \]

• Electronic stopping – interaction of incident ion with the cloud of electrons surrounding the target atoms
  \[ S_e(E) = \frac{dE}{dx} \]

Average rate of energy loss with distance

\[ \frac{dE}{dx} = S_n(E) + S_e(E) \]

range \[ R = \int_{x_0}^{x_f} dx = \int_{x_0}^{x_f} \frac{dE}{S_n(E) + S_e(E)} \]

Collision of hard spheres.

Projected range

\[ R_p \approx R \left( \frac{M_1}{M_1 + M_2} \right) \]

Projected straggle

\[ \sigma_p \approx \frac{2}{3} \left( \frac{M_1 M_2}{M_1 + M_2} \right) R_p \]
Implantation Damage (Disorder & Annealing)

- Estimated dose required to convert a crystalline material to an amorphous material
- The heavily damaged polycrystalline state in GaAs makes this material semi-insulating with an active carrier concentration < $10^{11}$ cm$^{-3}$.
- Material parameters are degraded – mobility, lifetime
- Implanted ions (most) are not in substitutional sites

Material Resistivity

- Quartz $\approx 10^{18}$ $\Omega$-cm (insulator)
- Silicon (Si) & gallium arsenide (GaAs) $\approx 1$ $\Omega$-cm (semiconductor)
- Silver $= 10^{-6}$ $\Omega$-cm (conductor)
Resistivity, Conductivity

Ohm’s Law: $J = \sigma E = \frac{1}{\rho} E$

- $J =$ the current density \((A/cm^2)\)
- Current density is proportional to the E-field
- \(\rho = \text{resistivity} \cdot \Omega \cdot \text{cm}\)
- \(\sigma = \text{conductivity} \cdot \Omega^{-1} \cdot \text{cm}^{-1}\)

**Derivation**

**Electric field:**

\[ E = \frac{1}{q} \frac{dE_C}{dx} \text{ (V/cm)} \]

**Electron current** $I_e = qnA\mu\, v_e = -\mu_e E$

**Sheet-Resistance Definition**

Resistance $R$ of the rectangular block of uniformly doped material shown below

\[ R = \rho L \quad \text{Area} = tW \]

where \(\rho = \text{material's resistivity}\)

- $L =$ length of block
- $A =$ cross-sectional area of block

where $R_s = \left( \frac{\rho}{t} \right)$ is called the **sheet resistance** of the layer of material

\[ \rho = \left( \frac{1}{\sigma} \right) \quad \text{and} \quad \sigma = q(\mu_n n + \mu_p p) \]

**Sheet resistance** of a material is the ratio of resistivity to thickness

Top and side views of two diffused resistors of different physical size having equal values of $R$. Each resistor has a ratio $L/W$ equal to 7 squares. Each end of the resistor contributes approximately 0.65 additional squares
Problem: Calculate the RC time constant for a 1 cm long doped polysilicon interconnection runner on 1 µm thick SiO₂. The polysilicon has a thickness of 5000 Angs. and a resistivity of 1000 µΩ-cm.

Soln:

NOTE:
As width of line ↑, RC ↓
As line length ↑, RC ↑

Four-Point Probe Measurement

Four-point probe with probe spacing s used for direct measurement of bulk wafer resistivity and the sheet resistance of thin diffused layers. A known current is forced through the outer probes, and the voltage developed is measured across the inner probes.

\[ \rho = \frac{2\pi s (V / I)}{\rho \pi} \quad \Omega \text{-cm} \quad t >> s \]

\[ \rho = \frac{(\pi t / \ln 2)(V / I)}{\rho \pi} \quad \Omega \text{-cm} \quad s >> t \]

For shallow layers:

\[ R_s = \frac{\rho}{t} = \frac{(\pi / \ln 2)V}{I} = 4.53V/I \quad \Omega \text{-cm} \quad s >> t \]

\[ \rho = F \rho_{\text{measured}} \]
Measuring Resistivity - Four-Point Probe Measurement

Four-Point probe Method:

Key features

• Probes equally spaced
• Small current I passed through outer probes
• Voltage V measured between inner probes

Thin semiconductor with thickness (w) much smaller than sample diameter (d)

Resistivity is given by:

\[ \rho = \frac{V}{I} \cdot W \cdot CF \ \Omega \cdot cm \]

where

CF = “correction factor”, depends on ratio of d/s where s is the probe spacing

When \( \frac{d}{s} > 20 \), \( CF \approx 4.54 \)

Measurement of resistivity using a four-point probe.

MEMS Fabrication

• Bulk micromachining
• Surface micromachining – constructed entirely from thin films
• LIGA – lithographic, galvanofomung, abformung
  – Consists of three basic processing steps:
    • Lithography, Electroplating, Molding
    • Based upon X-ray radiation
    • Can produce microstructure with lateral dimensions in the micrometer range & structural heights of several hundred micrometers from a variety of materials

Fabrication process of simple silicone rubber membrane. (a) Nitride deposition and patterning; (b) KOH etching; (c) silicone rubber spin coating; and (d) nitride removal on back side.
LIGA Fabrication Process

If you want a good ohmic contact on Si:
1) Put metal on with silicide
2) Put metal over highly doped region

Micro Wirebonding Process

Sequence of nail head bonding steps.
Profilometer Measurement – Step profile

Measurement technique to determine relative thickness of deposited or evaporated film

![Image of profilometer](image.png)

Chemical Mechanical Polishing (CMP)

Three main parts of the CMP process
- Surface to be polished
- The pad – key media enabling the transfer of mechanical action to the surface being polished
- The slurry – provides both chemical and mechanical effects

![Image of CMP process](image.png)

Figure 11.23. Process sequence used to fabricate a Cu line-stud structure using dual damascene. (a) Resist stencil applied; (b) reactive ion etching dielectric and resist patterning; (c) trench and via definition; and (d) Cu depositions followed by chemical-mechanical polishing (CMP).

Figure 11.24. A schematic of a CMP polisher.
Fabrication Summary

- Semiconductor Materials
- Crystal Structure
- Crystal Growth
  - Czochralski
  - Brigman
- Miller indices
- Epitaxy
- Film Formation
- Deposition
- Metalization
- Lithography
- Etching
  - Dry
  - Wet
- Doping
  - Diffusion
  - Implantation
- Resistivity
- Other useful techniques