Digital Controller Design Using Root Locus

- One may regard the design of a control system by the root locus method as a pole-placement problem solved by trial-and-error. In other words, the root-locus design essentially involves the determination of the system and controller parameters so that the roots of the characteristic equation are at the desired locations.

- For systems with an order higher than third, it is generally very difficult to establish a relation between the controller parameters and the C.E. roots.

- Furthermore, the conventional root locus diagram only allows one parameter to vary at a given time. Therefore, the design of a digital control system in the z-plane using a root locus diagram is essentially a trial-and-error method. Or, the designer may rely on a digital computer to plot out a large number of root loci by scanning through a wide range of possible values of the controller parameters and select the best solution.

- However, the experienced designer can still make proper and intelligent initial “guesses” so that the amount of trial-and-error effort is kept to a minimum.

- Therefore, it is useful to investigate the effects of the various pole-zero configurations of the digital controller on the overall system performance and the characteristic equation roots.
Phase-Lag and Phase-Lag Controllers

- Let us consider the first-order controller transfer function
  \[ D(z) = K \frac{z - z_1}{z - p_1} \]
  where \( z_1 \) is a real zero and \( p_1 \) is a real pole. In general, if the digital controller is to not affect the steady-state performance of the system, we set
  \[ \lim_{z \to 1} D(z) = 1 \]
  Therefore, we get
  \[ K = \frac{1 - p_1}{1 - z_1} \]

- In general, we may have a phase-lag controller with one pole in the right-half and one zero in the left-half of the \( z \)-plane, both inside the unit circle, or both the pole and the zero on the negative real axis inside the unit circle, with the pole located to the right of the zero. However, these configurations are generally not as effective in stabilizing a system as the "dipole" arrangement as shown below.

Pole zero configuration of a phase-lag controller as a "dipole" in (a) the \( s \)-plane (b) the \( z \)-plane.
• For a phase-lead controller (high pass filter) in the s-plane, the zero is always to the right of the pole on the negative real axis in the s-plane.

• The same is true for the relative pole-zero location of $D(z)$ in the z-plane. Figure below illustrates three possible pole-zero configurations of $D(z)$ as a first-order high pass filter.

• The following examples illustrate typical digital control system design problems carried out in the z-plane using the root locus technique.
Example 1: Consider that the controlled process of the digital control system shown in Fig. 1 is described by the transfer function

\[ G_p(s) = \frac{K}{s(1+0.15)(1+0.5s)} \text{, } T = 0.5 \text{ secs} \]

The problem involves the design of the digital controller so that the following set of performance specifications are met:

(i) ramp error constant \( K_v > 1.4 \)

(ii) relative damping ratio of the dominant root \( \zeta \geq 0.707 \)

\[ G(s) \]

\[ C(s) \]

\[ C(s) \]

\[ G_p(s) \]

\[ G(s) \]

\[ D(z) \]

\[ Z.O.H. \]

\[ G_p(z) \]

\[ C(z) \]

\[ Z(s) \]

\[ R(s) \]

\[ E(s) \]

\[ H(s) \]

\[ G(s) = G_{po} G_p(s) = (1-e^{-ST}) \frac{K}{s(1+0.15)(1+0.5s)} \]

\[ \therefore G(z) = G_{po} G_p(z) = \left(1-\frac{z^{-1}}{1-0.15}ight) \frac{K}{s(1+0.15)(1+0.5s)} \text{, } T = 0.5 \]

\[ = K \frac{0.13(z+1.3147)(z+0.0952)}{(z-1)(z-0.0067)(z-0.3679)} \]  \( \ldots (1) \)

Let us set the ramp error constant \( K_v \) to be at 1.4, therefore

\[ K_v = 1.4 = \lim_{z \to 1} \frac{1}{T} (z-1) G_{po} G(z) \]

\[ = 2.0 \frac{0.13K(2.3147)(1.0452)}{(0.9933)(0.321)} \]

\[ = \frac{1.4(0.9933)(1.0452)}{0.26(2.3147)(1.0452)} = 1.4 \]
The root locus diagram of the open-loop transfer function given in equation (1) is shown in Figure 2. Figure 2 also shows the spiral for $s = 0.707$ and the $K$ values for $s = 0.707$ and for marginally stable system. It can be seen from figure 2 that to satisfy the damping ratio specification, $K$ should be $0.585$, however, to satisfy the ramp error constant specification, $K$ should be $1.4$. Therefore, the uncompensated system cannot satisfy both the specification and hence we need to design a digital controller. The problem is to find a digital controller which will realize $K = 1.4$ and $s = 0.707$ simultaneously.

- It can be seen from Figure 2 that the damping ratio requirement can be satisfied if $K$ is set to $0.585$. This means that we do not have to reshape the root loci, and only the system gain $K$ has to be modified. But, we simply cannot just lower the value of $K$. Therefore, we need a controller which will raise the loop gain effectively, but at the same time does not alter the pole-zero configuration of the overall system appreciably. The phase lag controller with a “dipole” discussed earlier satisfy this requirement.

Let us introduce a phase-lag controller with the transfer function

$$D(z) = K_c \frac{z - z_1}{z - p_1}$$

where

$$K_c = \frac{1 - p_1}{1 - z_1}$$

- Most important, we stipulate that the value of $z_1$ and $p_1$ should be very close together, and that they are also very close to 1 (but less than 1). Also, $z_1$ is less than $p_1$. 
Figure 2. Root loci of the uncompensated digital control system in example 1.
• The main purpose of $D(z)$ is to introduce the attenuation $K_c = \frac{1-p_1}{1-z_1}$. Once this principle is established, the design becomes extremely simple, because all we have to do is set $K_c$ to the ratio of $\frac{0.585}{1.4}$, which is the ratio of the gain to realize $s = 0.707$ and the gain to realize $K_v = 1.4$, i.e.,

$$K_c = \frac{1-p_1}{1-z_1} = \frac{0.585}{1.4}$$

• However, we have one equation with two unknowns in this last equation. We have yet to apply the condition that $p_1 = z_1 = 1$ and $z_1 < p_1 < 1$.

• Setting $p_1$ arbitrarily to 0.99, we get

$$\frac{1-0.99}{1-z_1} = \frac{0.585}{1.4}$$

$$\therefore z_1 = 0.976$$

Thus, we have

$$D(z) = 0.418 \frac{z-0.976}{z-0.99} = \frac{0.418z-0.408}{z-0.99}$$

• Since the "dipole" is located very near the $z=1$ point, the root loci at a distant relatively far from $z=1$ are not affected in any significant way by the addition of the "dipole," and the only effect is that the loop gain of the system is changed by $K_c$. Figure 3 shows the root loci of the compensated system and the uncompensated system.

• It is important to note that the absolute values of $p_1$ and $z_1$ are not important, so long as they are close to one. However, the ratio of $\frac{1-p_1}{1-z_1}$ is important and must be set according to the amount of attenuation desired in the loop in order to achieve the desired damping.
Figure 3. Root loci of the uncompensated and compensated digital control system in example 1.
The closed-loop transfer function of the compensated system is given by

\[
\frac{C(z)}{R(z)} = \frac{D(z) G(z)}{1 + D(z) G(z)}
\]

\[
= \frac{0.918 \left( \frac{z - 0.976}{z - 0.99} \right) \left( \frac{1.43 \times 0.13}{(z - 0.0067)(z - 0.3679)} \right)}{1 + D(z) G(z)}
\]

\[
= \frac{0.0777(z + 1.3147)(z - 0.976)(z + 0.0452)}{(z + 0.0043)(z - 0.9748)(z^2 - 1.3164z + 0.4944)}
\]

\[
= \frac{0.0777(z + 0.3839z^2 - 1.2678z - 0.058)}{z^4 - 2.2869z^3 + 1.7678z^2 - 0.4743z - 0.0021}
\]

The step response of the compensated system is shown in Figure 4. It can be seen that the maximum overshoot is approximately 9%. Which is slightly more than 5% desired. The overshoot can be reduced by decreasing the K value to 1.4.

- One of the problems with the phase lag control is the response time of the compensated system. It takes more than 15 secs for the system response to be within 2% of the final value. This is an inherent problem with a phase lag controller (low pass filter). To speed up the system response, we need to design a phase-lead controller.
Figure 4. Step response of the compensated system in example 1.
• With phase-lag compensation, numerical problems may occur in the realization of the filter coefficients. To illustrate this point, suppose that a microprocessor is used to implement the digital controller. Suppose, in addition, that filter coefficients are realized by a binary word that employs 8 bits to the right of the binary point. Then the fractional part of the coefficient can be represented as

\[
\text{fraction} = b_7 \times \frac{1}{2} + b_6 \times \frac{1}{4} + b_5 \times \frac{1}{8} + b_4 \times \frac{1}{16} + \ldots + b_0 \times \frac{1}{256}
\]

where \(b_i\) is the \(i\)th bit and has a value of either 0 or 1. For example, the binary number

\[
0.11000001 = \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{256}\right)_{10} = (0.75390625)_{10}
\]

The maximum value that the fraction can assume is \(1 - \frac{1}{256}\) or 0.99609375.

Let us take the example of the following digital controller

\[
D(z) = \frac{0.3891z - 0.3884}{z - 0.9993}
\]

The numerator coefficients, when converted by standard decimal-to-binary conversion algorithms becomes

\[
(0.3891)_{10} \Rightarrow (0.011000011)_{2} = 0.3867185
\]

\[
(0.3884)_{10} \Rightarrow (0.011000011)_{2} = 0.3867185
\]
Thus, the compensator zero has been shifted to \( z = 1 \), and the digital controller that is implemented has the transfer function

\[
D(z) = \frac{0.3867185(z-1)}{z-0.99609375}
\]

- It can be seen that the implemented filter has a dc gain of zero; thus the system will not respond correctly to a constant input.
- Hence, more bits must be used to represent the filter coefficients.
Example 2: Offline controller design by trial and error will be illustrated in this example. Consider the system of Example 1.

Solution: The open-loop transfer function of the uncompensated system is given by

$$G(z) = K \frac{0.13(z+1.3147)(z+0.0452)}{(z-1)(z-0.0067)(z-0.3679)}$$

We will design a phase-lead compensator with a zero set at 0.3679, in order to cancel one of the plant pole. We will place the controller pole at $z = -0.7$, which should increase the system speed of response. Then

$$D(z) = K_c \frac{z-z_1}{z-p_1} = 2.69 \frac{z-0.3679}{z+0.7}$$

Note that $K_c = 2.69$ such that $D(1) = 1$. The root locus of the compensated system is shown in Figure 5.

Root locus of the uncompensated system is also shown in Figure 5. It can be seen from Figure 5 that the root locus of the compensated system is shifted to the left when phase-lead controller is added to the system and hence the system stability is increased. Therefore, by adjusting the value of $p_1$ within the unit circle (to the left of the zero), a desired root locus can be obtained.

For the digital controller described above, the value of $K$ for $s = 0.707$ is obtained as 1.47. The closed-loop transfer function of the compensated system is given by (let us use $K = 1.44$ for overdesign).
Figure 5. Root locus of the uncompensated and compensated systems in example 2.
\[
\frac{C(z)}{R(z)} = \frac{D(z)G(z)}{1 + D(z)G(z)} = \frac{2.69 \frac{z - 0.3619}{z + 0.7}}{\frac{1.4 \times 0.13(z + 1.3147)(z + 0.0452)}{\left(z - 1\right)(z - 0.0067)(z - 0.3694)}} \]

\[
= \frac{0.4896(z + 1.3147)(z + 0.0452)}{z^3 + 0.1829z^2 - 0.322z + 0.0338}
\]

The step response of the compensated system is shown in Figure 6. It can be seen from this figure that the overshoot is approximately 7%. The overshoot can be decreased by reducing the value of K. It can also be seen from this figure that it takes less than 3 secs to reach with 2% of the final value.

Figure 6. Unit Step response of the compensated system for example 2.
Example 3: Phase-Lag Controller Design for an Unstable System

The block diagram of a digital control system is shown in Figure 7. The controlled process is described by the transfer function

\[ G_p(s) = \frac{K}{s^2} \]

which may represent a pure inertial load.

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Figure 7. Block diagram of a digital control system.

The open-loop transfer function of the uncompensated system is

\[ G(z) = (1-z^{-1})^3 \left[ \frac{K}{s^2} \right] = \frac{KT^2(z+1)}{2(z-1)} \]

(1)

For this particular process, since \( T \) appears only as a multiplying factor in the open-loop transfer function, the root locus method can be applied to study the effects of variables \( K \) and \( T \) simultaneously. Figure 8 shows the root locus of the system based on the pre-zero configuration of the transfer function in equation (1). The variable parameter of the root loci is \( K' = KT^2 \). It is apparent that the system is unstable without a controller for any value of \( K' \).

Since \( G(z) \) has two poles at \( z=1 \), a phase-lag controller with a pole located to the right of its zero would simply push the loci further toward the right near \( z=1 \). Thus, it would seem logical to try a phase-lead controller. Let the transfer function of the phase-lead controller be

\[ D(z) = K_c \frac{z-z_1}{z-p_1} \]

where \( z_1 > p_1 \), and \( K_c = (1-p_1)/(1-z_1) \). To select the values of \( p_1 \) and \( z_1 \), we notice that it would be desirable to place the zero near two poles of \( G(z) \) at \( z=1 \). Figure 8 shows the root loci of the compensated system with \( z_1 = 0.95 \) and \( p_1 = 0.5 \). The transfer function of the controller is given by

\[ D(z) = 10 \frac{z-0.5}{z-0.95} \]

(2)
Figure 8. Root-locus of the uncompensated system and the compensated system with the controller $10(z-0.6)/(z-0.95)$ in example 3. The closed-loop system is now stable for $Kt^2 < 0.19$. Thus, if the sampling period is 0.1 sec, the marginal value of $K$ for stability would be 19.

It would be ideal if the zero $z$ could be placed at $z = 1$ to cancel one of the poles of $G(z)$; however, this would correspond to an infinite $K_c$.

In the above design, the pole $p_1$ was arbitrarily placed at 0.5. What would be the effect of moving $p_1$ along the real axis inside the unit circle? It is apparent that $p_1$ should not be placed too close to the zero at $z_1$, or the phase-lead controller would not be too effective in improving the stability of the system. On the other hand, the pole can be placed on the negative real axis within the unit circle. This corresponds to more phase-lead, since the distance between $z_1$ and $p_1$ is increased. Figure 9 shows the root loci when the digital controller has the transfer function

$$D(z) = 30 \frac{z-0.95}{z+0.5}$$ (3)
Now, when \( K' = 0.08 \), the closed-loop system has a damping ratio of approximately 0.707. The unit step responses of the compensated system with the two different controllers and two values of \( K' \) are shown in Figure 10. With the controller as described by equation (2) with \( z_1 = 0.95 \) and \( p_1 = 0.5 \), the unit step response has a maximum overshoot in excess of 60\% with \( KT^2 \) of 0.05. With the controller as described by equation (3) and \( K' = KT^2 = 0.038 \), the unit step response has a maximum overshoot of only 13\%. For the same controller with \( K' \) decreased to 0.025, the response is slower but the maximum overshoot is decreased to 8\%.

**Figure 9.** Root loci of the compensated system in example 3 with \( D(z) = 30 (z - 0.95)/(z + 0.5) \).
Figure 10. Unit step responses of the compensated digital control system in example 3.