Bipolar Junction Transistors (BJT)

PNP & NPN (Emitter Base Collector)

Note: NPN's are more commonly encountered due to greater ease of production.
Bipolar (majority and minority carriers)
Forward voltage characteristics of PN junction (approximately 0.2 volts for Ge and 0.7 volts for Si).

Biasing:

NPN $V_c > V_e$ $V_{be} = +0.7$ PNP $V_e > V_c$ $V_{be} = -0.7$

BJTs are current-controlled devices: Symbology and Voltage / Current Relationships:

V_{BB}	Base Bias Voltage	$I_e = I_c + I_b$
V_{EE}	Emitter Bias Voltage	$I_c = \alpha I_e$
V_{CC}	Collector Bias Voltage	$I_c = \beta I_b$
V_{be}	Voltage drop across Emitter Base Junction	$I_e = (1 + \beta) I_b$
V_{cb}	Voltage drop across Collector Base Junction	$I_b = (1 - \alpha) I_e$
V_{ce}	Voltage drop from Collector to Emitter	$\beta = \alpha(1 - \alpha)$
		$\alpha = \beta(1 + \beta)$
		$\alpha \approx 1$ $\beta = 20 - 2000$ (100 - 400)

Three Regions of BJT operations and required biasing for each:

Active (Linear) {Amplification}	Base Emitter Forward, Collector Base Reverse
Cut-Off {Open Switch - No Current Flow}	Base Emitter Reverse, Collector Base Reverse
Saturation {Closed Switch - High Current Flow}	Base Emitter Forward, Collector Base Forward

Active Region Linear Amplification (High Fidelity - No Distortion)
- Emitter/Base Forward Bias
- Collector/Base Reverse Bias

Cut-Off Region
- Both junctions reversed biased
  - Emitter/Base voltage insufficient to cause emitter current flow
  - Zero current (same as open switch)

Saturation Region
- Both junctions forward biased
  - Heavy current conduction (same as closed switch)

Configurations and Characteristics:

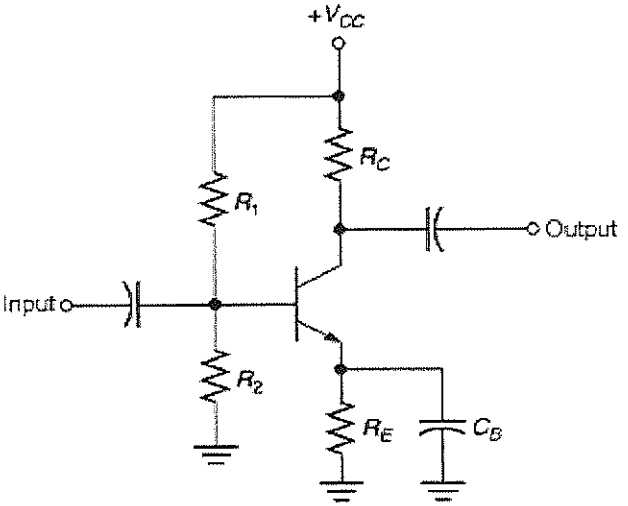
Common Base
- Unity Current Gain
- High Voltage Gain
- No phase shift

Common Emitter
- 180° Phase Shift
- High Power Gain (Both High Current and High Voltage Gains)
- Most frequently used configuration

Common Collector (Emitter Follower)
- Unity Voltage Gain
- No phase shift
- High Input Impedance & Low Output Impedance

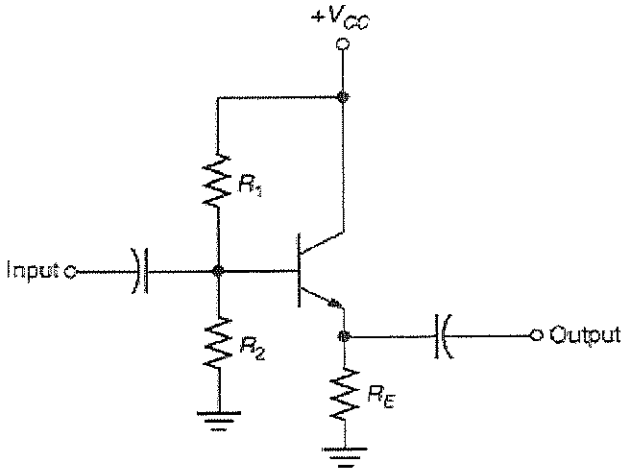
BJT Amplifiers

	Voltage Gain (Av)	Current Gain (Ai)	Power Gain (Ap = AvAi)	Input Impedance	Output Impedance	Phase Shift
Ideal	Infinite	Infinite	Infinite	Infinite	Zero	N/A
Common Emitter	100 - 1000	100 - 1000	> 1000	1 - 10K Ohm	1 - 10K Ohm	180°
Common Collector (Emitter Follower)	<1	100 - 1000	< Ai	> 10K Ohm	< 1K Ohm	0°
Common Base	100 - 1000	< 1	<Av	< 1K Ohm	> 10K Ohm	0°



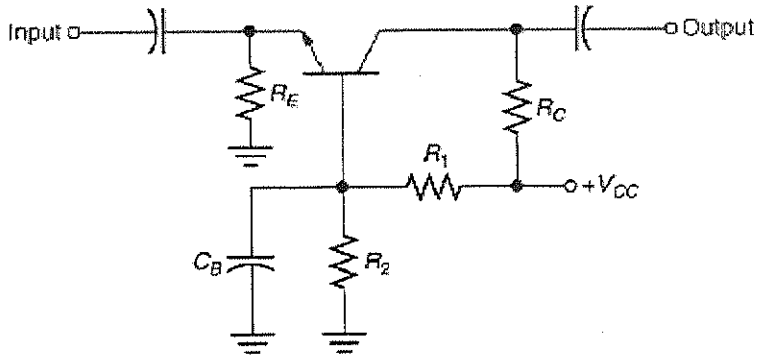
A common-emitter (CE) amplifier

(a)



A common-collector (CC) amplifier

(b)

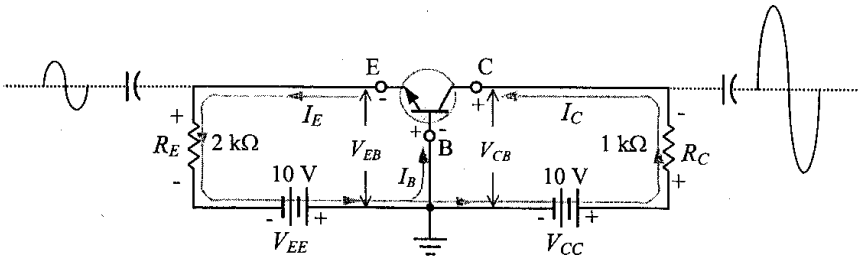


A common-base (CB) amplifier

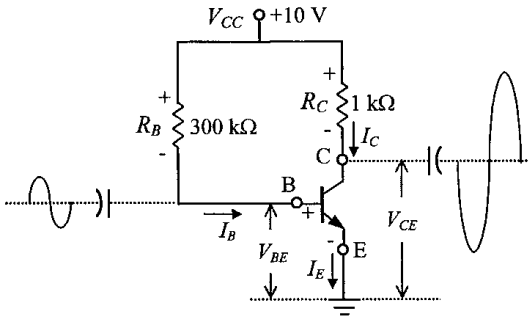
(c)

Robert T. Paynter
Introductory Electronic Devices and Circuits: Electron Flow Version, 6e

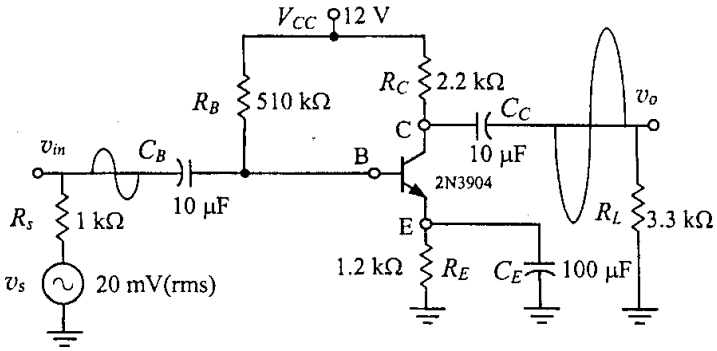
BJT Amplifier Configurations



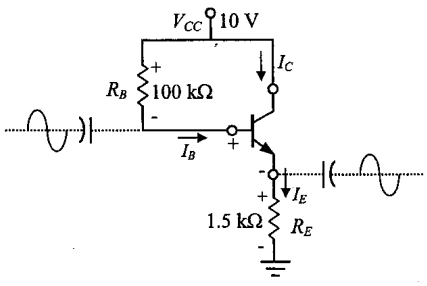
Common Base-Biased BJT Amplifier



Base-Biased Common Emitter BJT Amplifier

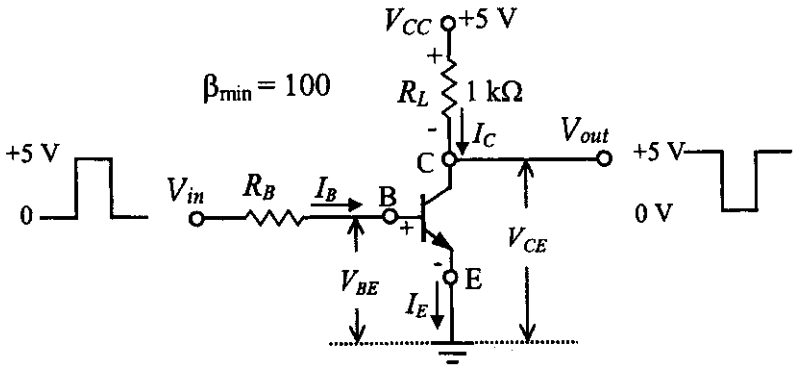


Emitter-Biased Common Emitter BJT Amplifier

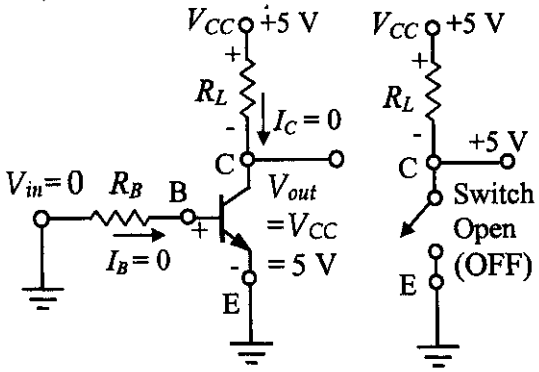


Emitter-Biased Common Collector BJT Amplifier

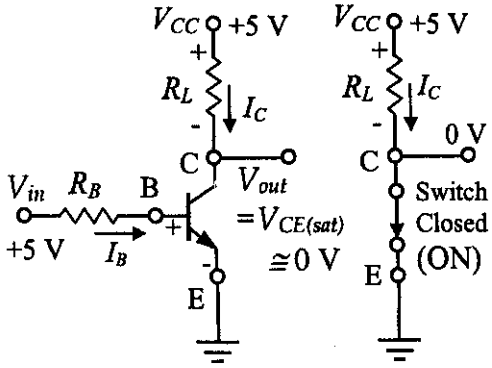
Transistor Switch



The BJT Inverter



Transistor OFF



Transistor ON

Field Effect Transistors (FET)

FET (JFET & MOSFET)

P-type & N-type (Source, Drain, Gate)

Unipolar (majority carriers only)

JFETs are voltage-controlled devices: $v_o = a v_i$

Forward Bias with respect Source & Drain

P Channel: Source + and Drain - (conventional current flow Source to Drain I_D)

N Channel: Source - and Drain + (conventional current flow Drain to Source I_D)

Reverse Bias with respect to Source & Gate (Max current flow I_D when $V_{gs} = 0$)

P Channel: Gate more positive than Source causes a decrease in I_D current flow

N Channel: Gate more negative than Source causes a decrease in I_D current flow

Terminology:

V_P (Pinch-Off Voltage)

The V_{DS} voltage at which the current I_D levels off (V_{GS}=0)

I_{DSS} (Drain-Source Saturation Current)

Maximum current flow with $V_{DS} > V_P$ and $V_{GS} = 0$.

$V_{GS(off)}$ (Gate-to-Source Cutoff Voltage) Note: $V_P = |V_{GS(off)}|$

The value of V_{GS} which results in total channel depletion, and hence zero current flow ($I_D = 0$).

Quiescent (Operating Points)

I_{DQ}

V_{DSQ}

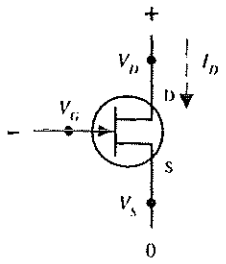
Equations:

Self Biased $\quad I_D = \frac{-V_{GS}}{R_S} \qquad V_{DS} = V_{DD} - I_D(R_D + R_S)$

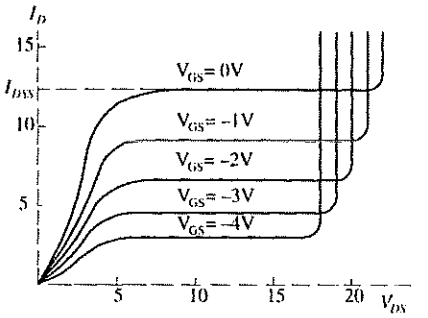
Voltage Divider $\quad I_D = \frac{V_G - V_{GS}}{R_S} \qquad V_{DS} = V_{DD} - I_D(R_D + R_S)$

Field Effect Transistors (FETS)

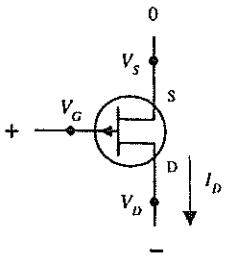
N-CHANNEL JFET



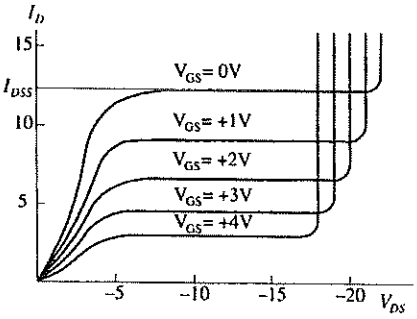
N-CHAN CURVES



P-CHANNEL JFET



P-CHAN CURVES



DRAIN CURRENT (OHMIC REGION)

$$I_D = I_{DSS}\left[2\left(1 - \frac{V_{GS}}{V_{GS,off}}\right)\frac{V_{DS}}{-V_{GS,off}} - \left(\frac{V_{DS}}{V_{GS,off}}\right)^2\right]$$

DRAIN CURRENT (ACTIVE REGION)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS,off}}\right)^2$$

DRAIN-SOURCE RESISTANCE

$$R_{DS} = \frac{V_{DS}}{i_D} \approx \frac{V_{GS,off}}{2I_{DSS}(V_{GS} - V_{GS,off})} = \frac{1}{g_m}$$

ON RESISTANCE

$$R_{DS,on} = \text{constant}$$

DRAIN-SOURCE VOLTAGE

$$V_{DS} = V_D - V_S$$

TRANSCONDUCTANCE

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|V_{DS} = \frac{1}{R_{DS}}$$

$$= g_{m_0}\left(1 - \frac{V_{GS}}{V_{GS,off}}\right) = g_{m_0}\sqrt{\frac{I_D}{I_{DSS}}}$$

TRANSCONDUCTANCE FOR SHORTED GATE

$$g_{m_0} = -\frac{2I_{DSS}}{V_{GS,off}}$$

Typical JFET values:

I_{DSS}: 1 mA to 1 A

$V_{GS,off}$:
–0.5 to –10 V (*n*-channel)
0.5 to 10 V (*p*-channel)

$R_{DS,on}$: 10 to 1000 Ω

BV_{DS}: 6 to 50 V

g_m at 1 mA:
500 to 3000 µmho

OHMIC REGION JFET is just beginning to resist. It acts like a variable resistor.

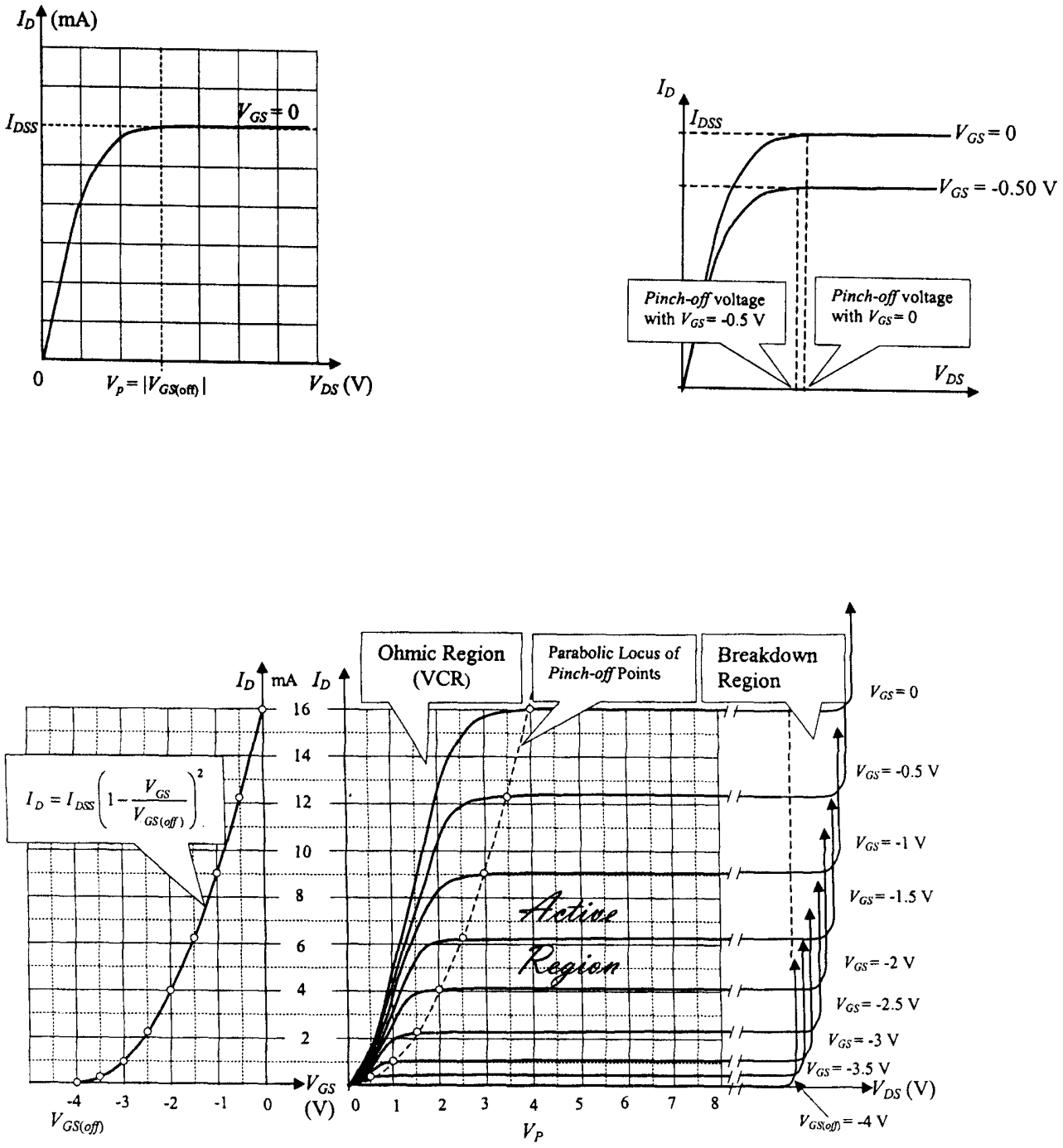
SATURATION REGION JFET is most strongly influenced by gate-source voltage, hardly at all influenced by the drain-source voltage.

CUTOFF VOLTAGE ($V_{GS,off}$) Particular gate-source voltage where JFET acts like an open circuit (channel resistance is at its maximum).

BREAKDOWN VOLTAGE (BV_{DS}) The voltage across the drain and source that caused current to "break through" the JFET's resistive channel.

DRAIN-CURRENT FOR ZERO BIAS (I_{DSS}) Represents the drain current when gate-source voltage is zero volts (or gate is connected to source, $V_{GS} = 0$ V).

TRANSCONDUCTANCE (g_m) Represents the rate of change in the drain current with the gate-source voltage when the drain-to-source voltage is fixed for a particular V_{DS}. It is analogous to the transconductance ($1/R_{tr}$) for bipolar transistors.



(b) Transfer Characteristics (a) Drain Characteristics

Figure 7-8: Plot of Drain and Transfer Characteristics for an *n*-channel JFET

Figures 7-6,7, 8. Kazimierczuk Electronic Devices

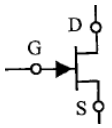
Source: Electronic Devices a design approach. Ali Aminian and Marian Kazimierczuk, 2004

Junction Field Effect Transistors JFET

Three Terminals: Drain, Source, Gate

Majority Carriers Only (Unipolar)
N Channel Electrons

By convention, always draw with **Drain** at the top



N Type Channel Arrow Pointing **IN**

Forward Bias Source to Drain V_{DD}

For N Channel
+ to Drain
- to Source
Conventional Current Flow I_D (From Drain to Source)

Reverse Bias Gate to Source $I_G = 0$
- to Gate
+ to Source

V_G is the Gate to Ground Voltage
V_{GS} is the Gate to Source Voltage

V_P (Pinch-Off Voltage) The V_{DS} voltage at which the current I_D levels off (for $V_{GS} = 0$)

$V_{GS(off)}$ (Gate-to-Source Cutoff Voltage $I_D = 0$) $V_P = |V_{GS(off)}|$

I_{DSS} (Drain-Source Saturation Current) Maximum current flow with $V_{GS} = 0$.

Quiescent (Operating Points)

I_{DQ}

V_{DSQ}

Shockley's Equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Notes:

V_{GS} and $V_{GS(off)}$ are always the same algebraic sign, so $V_{GS} / V_{GS(off)}$ will always be positive.

For N Channel, $V_{GS(off)}$ is negative, $V_P = |V_{GS(off)}|$, so $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$

Biasing N Channel JFETs i.e., calculating Quiescent (Operating Points), I_{DQ} and V_{DSQ}

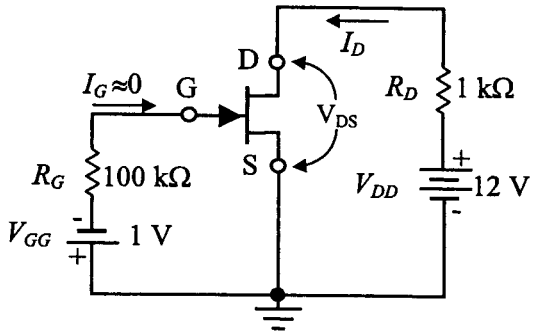
I_{DSS} and $V_{GS(off)}$ are from readily obtainable from Transfer Characteristics Charts

For Fixed Biased, $V_{GS} = V_{GG}$ (since reversed bias, $I_G = 0$, $V_{RG} = 0$, $V_{GS} = V_{GG}$)

For Self Biased and Voltage Divider Biased, V_{GS} is the solution of a quadratic equation.
For BME 3512, I_{DSS}, $V_{GS(off)}$, V_{GS} will be given.

Fixed Biased

I_{DSS} = 12 mA $V_{GS(off)} = -4$ V



A fixed bias circuit

Given: I_{DSS} = 12 mA $V_{GS(off)}$ = -4 V

Since Gate to Source is reverse biased, $I_G = 0$, hence $V_{Rg} = I_G R_g = 0$

And $V_{GG} = I_G R_g + V_{GS}$

$V_{GG} = 0 + V_{GS}$

$V_{GS} = V_{GG} = -1$ V

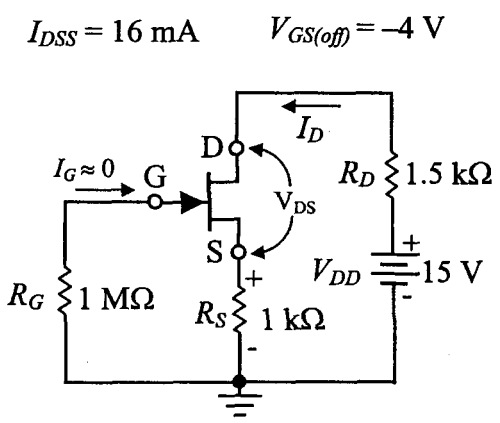
From Shockley's Equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 12\times10^{-3}\times\left(1 - \frac{-1}{-4}\right)^2 = 6.75 \text{ mA}$$

$$V_{DD} = V_{DS} + I_D R_D \rightarrow V_{DS} = V_{DD} - I_D R_D = 12 - 6.75\times10^{-3}\left(1\times10^{-3}\right) = 5.25 \text{ V}$$

Answers: I_{DQ} = 6.8 mA and V_{DSQ} = 5.3 V

Self-Biased



A self-biased circuit

Given: I_{DSS} = 16 mA $V_{GS(off)}$ = - 4 V V_{GS} = see below

The I_D current through R_S will develop a voltage across R_S such that the Source is at a positive potential with respect to Ground. If any current I_G flows at all, the Gate will be at a negative potential with respect to Ground and hence the Gate to Source will be reversed bias resulting in
$I_G = 0$, hence $V_{Rg} = I_G R_g = 0$, and therefore V_G (Gate to Ground) = 0.

But $V_G = V_{GS} + I_D R_S$

$0 = V_{GS} + I_D R_S$

$I_D = -V_{GS} / R_S$

From $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$ and $I_D = -V_{GS} / R_S$ $\rightarrow$ $\frac{-V_{GS}}{R_S} = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

Solve for V_{GS} (see page 5 Summary of FET Biasing Equations) Note:

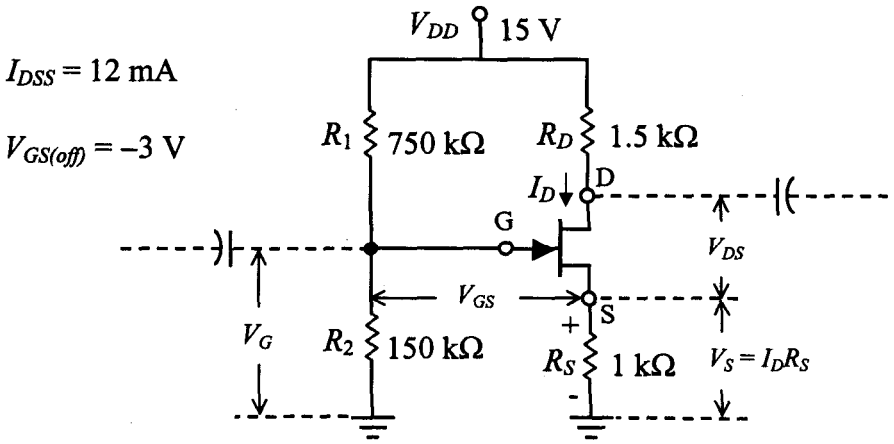
For BME 3512 the value of V_{GS} will be given. V_{GS} = - 2.44 V

$I_D = -V_{GS} / R_S$ = - (-2.44) / 1 x 10^3 = 2.44 mA

$V_{DD} = V_{DS} + I_D(R_D + R_S) \rightarrow V_{DS} = V_{DD} - I_D(R_D + R_S) = 15 - 2.44\times10^{-3}(1500+1000) = 8.9$ V

Answers: I_{DQ} = 2.4 mA and V_{DSQ} = 8.9 V

Voltage Divider Biased



A voltage-divider biased JFET amplifier circuit

Given: I_{DSS} = 12 mA $V_{GS(off)}$ = - 3 V V_{GS} = see below

From the voltage divider network: $V_G = V_{DD} \dfrac{R_2}{R_1 + R_2}$

By definition: $V_{GS} = V_G - V_S = V_G - I_D R_{SS}$

Hence $I_D = (V_G - V_{GS}) / R_S$

From $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)^2$ and $I_D = (V_G - V_{GS}) / R_S$ ➡ $\dfrac{V_G - V_{GS}}{R_S} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)^2$

Solve for V_{GS} (see page 5 Summary of FET Biasing Equations)

Note: For BME 3512 the value of V_{GS} will be given. V_{GS} = - 1.31 V

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2} = 15 \frac{150\,\text{K}}{750\,\text{K} + 150\,\text{K}} = 2.50\ \text{V}$$

$I_D = (V_G - V_{GS}) / R_S = [2.5 - (-1.31)] / 1000 = 3.81$ mA

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 15 - 3.81 \times 10^{-3}(1500 + 1000) = 5.48\ \text{V}$$

Answers: I_{DQ} = 3.8 mA and V_{DSQ} = 5.5 V

Summary of Equations for the Analysis of Self-Biased and Voltage-Divider Biased JFET Amplifier

Self-bias:

$$V_{GS}\Big|_{n-channel} = \frac{-b+\sqrt{b^2-4ac}}{2a}$$

$$V_{GS}\Big|_{p-channel} = \frac{+b-\sqrt{b^2-4ac}}{2a}$$

where,

$$a = \frac{I_{DSS}R_S}{V_P^{\,2}} \qquad b = \frac{2I_{DSS}R_S}{|V_P|}+1 \qquad c = I_{DSS}R_S$$

$$I_D = \frac{-V_{GS}}{R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Voltage-divider bias:

$$V_{GS}\Big|_{n-channel} = \frac{-b+\sqrt{b^2-4ac}}{2a}$$

$$V_{GS}\Big|_{p-channel} = \frac{+b-\sqrt{b^2-4ac}}{2a}$$

where,

$$a = \frac{I_{DSS}R_S}{V_P^{\,2}} \qquad b = \frac{2I_{DSS}R_S}{|V_P|}+1 \qquad c = I_{DSS}R_S - |V_G|$$

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Source: Electronic Devices a design approach. Ali Aminian and Marian Kazimierczuk, 2004