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1 Introduction

The VN-100 DEV is a development board for VN-100 attitude and heading reference module. It is designed to provide easy access to the module for development purposes. USB and RS-232 interfaces are provided, along with a header that includes full prototyping access to the VN-100.

The board can be powered by the USB host computer, a 5 V adapter, or through the 20 pin header. A red LED indicates the power status of the board.

The VN-100 North, East, Down coordinate system is shown in the mechanical drawings section.

Figure 1 – Development Board
2 Board configuration

2.1 Jacks

2.2 USB
The USB jack is a USB-B port. When connected to a PC the VN-100 DEV board will power up and a RED status LED will be illuminated. Drivers for the USB to UART must be installed for proper operation of this port. These are supplied with the documentation for the board or they can be downloaded at www.vectornav.com.

2.3 DB-9
The DB-9 port provides access to RS-232 level logic. The RS-232 line driver supports speeds up to 1 Mbit. The RS-232 interface requires the VN-100 DEV board to be powered to function properly. The power can be supplied thru the USB port or thru the 5V power jack.
2.4 **Power Jack**
This is a standard 5V power jack. This powers the board when using the RS-232 interface.

Warning: Do not exceed 6V input power.

2.5 **Indicator lights**

2.5.1 **Red LED**
Turns bright red when power is supplied to the board.

2.5.2 **Green LED’s**
These LED’s will flash when data is being transferred across USB. When using the RS-232 logic interface, neither the RX nor the TX LED on the silkscreen will flash. This is normal behavior and does not indicate that the board is not receiving/transmitting data.

2.6 **Push Buttons**

2.6.1 **S1/REPRGM**
S1 is only used to enable the VN-100 Boot mode. Depressing this switch during power-up, or reset of the VN-100 module will set the VN-100 into boot mode.

2.6.2 **S2/NRST**
S2 is used for re-setting the VN-100. Depressing S2 at any time while the board is running will reset the VN-100 module.

2.6.3 **S3/TARE/RESTORE**
S3 is normally used to tare the VN-100. To tare, pulse high for at least 1 μs. During power on or device reset, depressing S3 will cause the module to restore its default factory settings. Because of this, this button cannot be used for tare until at least 10 ms after a power on or reset.

2.7 **Jumpers**

2.7.1 **JP1**
JP1 toggles the TX (data leaving the VN-100 module) UART data line. With the jump between pin 1 and pin 2 the TX signal is routed to the RS-232 interface. Setting the jump to pin 2 and pin 3 enables the TX at the USB interface.

2.7.2 **JP2**
JP2 toggles the RX (data entering the VN-100 module) UART data line. With the jump between pin 5 and pin 6 the RX signal is routed to the RS-232 interface. Setting the jump to pin 4 and pin 5 enables the RX at the USB interface.
2.7.3 **J5 – Header**

The J5 header provides a complete interface to all the used pins on the VN-100 module.

### Table 1 – 20-Pin Header

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Description</th>
<th>Pin on VN-100</th>
<th>Note:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vcc (3.3-5.5V)</td>
<td>10</td>
<td>Power can only be supplied to the board and VN-100</td>
</tr>
<tr>
<td>2</td>
<td>REPRGM</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>TARE/RESTORE</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>NRST</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>ENABLE</td>
<td>11</td>
<td>ON state. Pull low to enter sleep mode</td>
</tr>
<tr>
<td>6</td>
<td>Not Used</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>TX</td>
<td>12</td>
<td>Data leaving VN-100 (UART 0/3.0V)</td>
</tr>
<tr>
<td>8</td>
<td>SPI_CS</td>
<td>23</td>
<td>SPI slave select</td>
</tr>
<tr>
<td>9</td>
<td>RX</td>
<td>13</td>
<td>Data entering VN-100 (UART 0/3.0V)</td>
</tr>
<tr>
<td>10</td>
<td>Not Used</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Not Used</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>DR_INT</td>
<td>9</td>
<td>Data Ready Interrupt. Will pulse low for 500 us</td>
</tr>
<tr>
<td>13</td>
<td>Not Used</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>(1-4)</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>SPI_SCK</td>
<td>16</td>
<td>SPI clock</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>(1-4)</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>SPI_MOSI</td>
<td>17</td>
<td>SPI master output/slave input</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>(1-4)</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>SPI_MISO</td>
<td>19</td>
<td>SPI master input/slave output</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>(1-4)</td>
<td></td>
</tr>
</tbody>
</table>
3 Mechanical Drawings

Figure 3 – Board Dimensions
4 Revision history

Table 2 – Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jun-05-2009</td>
<td>1.0.0</td>
<td>Initial release.</td>
</tr>
<tr>
<td>Oct-06-2009</td>
<td>1.1.0</td>
<td>New document format.</td>
</tr>
</tbody>
</table>
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